IEE  6703

ANALOG INTEGRATED CIRCUITS (I)

Lecture Note

CHUNG-YU WU

Integrated Circuits and Systems Laboratory
Department of Electronics Engineering
National Chiao Tung University
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IEEE 6703 ANALOG INTEGRATED CIRCUITS (I)

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Course Contents:

1. Analog MOSFET Device Physics and SPICE Models
2. CMOS Process Technology and Layout Rules
3. Current Sources and Simple Voltage Sources
4. Amplifiers, Level Shifting Circuits, and Output Stages
5. Noise Analysis of Analog Amplifiers
6. Midband Analysis of Operational Amplifiers (OP AMPs)
7. Frequency Response of Analog ICs
8. Design Procedures of CMOS OP AMPs
9. Special-Purpose CMOS OP AMPs
10. Passive Components and MOS Switches
11. Bandgap References
12. Sample and Hold Circuits

Text Book:


References:

2. Roubik Gregorian, Introduction to CMOS OP AMPs and Comparators, John Wiley & Sons, 1999
4. Technical Papers

**Final Scores:**

Will be determined by

(1) Homework 20%
(2) Mid-Term Test 30%
(3) Final Exam 30%
(4) Chip Design Project 20% (This Semester)
20% (Next Semester)

**Chip Design Schedule:**

Presimulation Deadline: : Dec. 4, 2000
Layout Deadline : Dec. 25, 2000
Post-Simulation Deadline : Jan. 8, 2001
Tapeout :

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Chapter 1  Device Physics and SPICE Models of Analog MOSFETs

§1-1 Device Physics and Operational Principle

Fig.1  Cross-sectional view of a n-channel MOSFET.

Fig.2  $I_{DS}$-$V_{DS}$ characteristics of long-channel NMOSFET.
Linear Region (Non-saturation Region) :

\[ V_{GS} > V_{THO} \] (threshold voltage)
⇒ electron inversion layer (~200Å) is formed
⇒ For small \( V_{DS} \), it likes an uniform resistor with length \( L_{eff} \), width \( W_{eff} \), and thickness 200 Å
⇒ Linear \( I_{DS} - V_{DS} \) curve
\[ I_{DS} = (\mu \frac{V_{DS}}{L_{eff}}) \left[ C_{OX} W_{eff} (V_{GS} - V_{THO}) \right] = \mu C_{OX} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{THO}) V_{DS} \]
⇒ For slightly larger \( V_{DS} \),
\[ I_{DS} = (\mu \frac{V_{DS}}{L_{eff}}) \left[ C_{OX} W_{eff} (V_{GS} - V_{THO} - \frac{1}{2} V_{DS}) \right] = \mu C_{OX} \frac{W_{eff}}{L_{eff}} \left[ (V_{GS} - V_{THO}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

Saturation Region :
1. Pinched-off saturation in long-channel devices

\[ V_{DS} = V_{GS} - V_{THO} \]
⇒ \[ V_{DS} = V_{DSAT} \]
At $V_{DS} = V_{DSAT} = V_{GS} - V_{THO}$, the channel is pinched off ($V_{GD} = V_{THO}$).

$$I_{DS} = \frac{\mu C_{ox} W_{eff}}{2 L_{eff}} (V_{GS} - V_{THO})^2$$

When $V_{DS} > V_{DSAT}$, the pinched-off point of $V_{DSAT}$ along the channel is moved toward the source with a distance $\Delta L$ from the drain.

$\Rightarrow$ Within $\Delta L$, the electrons can be very quickly swept toward the drain region. Thus the current is not dependent upon the physical behavior of electrons within $\Delta L$.

$$\Rightarrow I_{DS} = \frac{\mu C_{ox} W_{eff}}{2 L_{eff} - \Delta L} (V_{GS} - V_{THO})^2$$

$$\approx \frac{\mu C_{ox} W_{eff}}{2 L_{eff}} (V_{GS} - V_{THO})^2$$

for $\Delta L \ll L$ (long-channel device)

$\Rightarrow$ constant current characteristics.

2. **Velocity saturation in short-channel devices**

In short-channel devices $L_{\text{drawn}} < 4 \mu m$, velocity saturation occurs before pinched-off.

\[ V_{SAT} = \mu \frac{V_{DSAT}}{L_{eff}} \]

\[ I_{DSAT} = \mu \frac{V_{DSAT}}{L_{eff}} \left[ C_{ox} W_{eff} (V_{GS} - V_{THO} - \frac{1}{2} V_{DSAT}) \right] \]
When $V_{DS} > V_{DSAT}$, the charges per unit channel length are increased by a factor of $\frac{L_{eff}}{L_{eff} - \Delta L}$ effectively.

$$I_{DS} = I_{DSAT} \frac{L_{eff}}{L_{eff} - \Delta L}, \quad V_{DS} \uparrow \Rightarrow \Delta L \uparrow \Rightarrow I_{DS} \uparrow$$

Fig. 3 $I_{DS}$-$V_{DS}$ characteristics of short-channel NMOSFET

$I_{DS}$-$V_{GS}$ characteristics:

depletion mode

enhancement mode
Device symbols:

**Enhancement-Mode MOSFET**

- **n-channel**
- **p-channel**

**Depletion-Mode**
- **n-channel**

§1-1.1 Threshold Voltage $V_{TH}$

$$V_{TH} = \phi_{MS} - \frac{Q_{SS}}{C_{OX}} + \phi_S + \frac{Q_B}{C_{OX}} = V_{FB} + \phi_S + \frac{Q_B}{C_{OX}} \\
V_{FB} \equiv \phi_{MS} - \frac{Q_{SS}}{C_{OX}} + V_{TH}^{+NMOS}$$

- $\phi_{MS}$: gate material to silicon potential barrier
- $Q_{SS}$: surface charge density (C/cm²)
- $\phi_S$: surface potential under strong inversion
- $\phi_S = 2 \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)$ or $\frac{2kT}{q} \ln \left( \frac{n_i}{N_D} \right)$
- $Q_B$: bulk charge density (C/m²)
- $Q_B^{+NMOS}$, $Q_B^{-PMOS}$
- $C_{OX}$: channel oxide capacitance per unit area

$$C_{OX} = \frac{\varepsilon_{siOx}}{T_{ox}} \quad C_{OX} \equiv 0.037\text{fF/μm}^2 \text{ for } T_{OX} = 100\text{Å}$$
<table>
<thead>
<tr>
<th>Gate Material</th>
<th>( \Phi_{MS}(V) )</th>
<th>( Q_{ox} )</th>
<th>( V_{FB}(V) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>-0.3</td>
<td>-0.03</td>
<td>-0.3</td>
</tr>
<tr>
<td>NMOS</td>
<td>-0.85</td>
<td>-0.33</td>
<td>-0.88</td>
</tr>
<tr>
<td>metal</td>
<td>-0.25</td>
<td>-0.023</td>
<td>-0.273</td>
</tr>
<tr>
<td>n\textsuperscript{+}-polysilicon</td>
<td>+0.80</td>
<td>+0.30</td>
<td>+0.777</td>
</tr>
<tr>
<td>p\textsuperscript{+}-polysilicon</td>
<td>+0.80</td>
<td>+0.30</td>
<td>+0.777</td>
</tr>
</tbody>
</table>

\[
Q_{hi} = \sqrt{2 \varepsilon_{si} q N_A \Phi_S \left( N_D \right)} \quad \text{for } V_{BS} = 0 \quad \text{i.e. zero substrate bias}
\]

\[
Q_{hi} = \sqrt{2 \varepsilon_{si} q N_A \left( \Phi_S - V_{BS} \right) \left( N_D \right)} \quad V_{BS} > 0 \quad \text{forward bias}
\]

\[
V_{TH} = V_{THO} + \text{GAMMA} \sqrt{\Phi_S} \left[ \sqrt{1 - V_{BS} / \Phi_S} - 1 \right] \quad V_{THO} \quad \text{zero-bias threshold voltage}
\]

\[
V_{TH} = V_{THO} + \text{GAMMA} \left[ \sqrt{\Phi_S - V_{BS}} - \sqrt{\Phi_S} \right] \quad \varepsilon_{si} \quad \text{permittivity of Si}
\]

\[
V_{TH} \text{ and } V_{THO}: \quad + (-) \quad \text {for enhancement NMOS (PMOS)}
\]

\[
\text{GAMMA} = \frac{1}{\text{Cox}} \sqrt{2 \varepsilon_{si} q N_A} \quad \text{GAMMA: body effect factor}
\]

Body Effect \cdot Substrate Bias Effect

\[
\left| V_{BS} \right| \uparrow \text{ forward bias } \Rightarrow V_{TH} \downarrow
\]

\[
\left| V_{BS} \right| \uparrow \text{ reverse bias } \Rightarrow V_{TH} \uparrow
\]

\[
\text{GAMMA} \cong 0.1 \text{ to } 1.0 \quad \text{GAMMA} \propto \sqrt{N_A}
\]

To obtain a large enough \( V_{THO} \) and a small GAMMA
\implies \text{implantation for threshold voltage adjustment on a small } N_A \left( N_D \right) \text{ sub. enhancement implant & depletion implant.}
Threshold Voltage Equation

\[
V_{th} = V_{dhox} + K_{1ox} \cdot \sqrt{\Phi_s - V_{beff}} - K_{2ox} V_{beff}
+ K_{1ox} \left( 1 + \frac{Nlx}{L_{eff}} - 1 \right) \sqrt{\Phi_s + \left( K_3 + K_{sb} V_{beff} \right) \frac{T_{ox}}{W_{eff}} + W_0 \Phi_s}
\]

\[
- D_{TTOw} \left( \exp \left( - D_{VT1w} \frac{W_{eff} \cdot L_{eff}}{2l_{rw}} \right) + 2 \exp \left( - D_{VT1w} \frac{W_{eff} \cdot L_{eff}}{l_{rw}} \right) \right) \left( V_{bi} - \Phi_s \right)
\]

\[
- D_{TTO} \left( \exp \left( - D_{VT1} \frac{L_{eff}}{2l_t} \right) + 2 \exp \left( - D_{VT1} \frac{L_{eff}}{l_t} \right) \right) \left( V_{bi} - \Phi_s \right)
\]

\[
\left( \exp \left( - D_{sub} \frac{L_{eff}}{2l_{so}} \right) + 2 \exp \left( - D_{sub} \frac{L_{eff}}{l_{so}} \right) \right) \left( E_{sub} + E_{sub} V_{beff} \right) V_{ds}
\]

\[
V_{dhox} = V_{dho} - K_1 \cdot \sqrt{\Phi_s}
\]

\[
K_{1ox} = K_1 \cdot \frac{T_{ax}}{T_{acm}}
\]

\[
K_{2ox} = K_2 \cdot \frac{T_{ax}}{T_{acm}}
\]

\[
l_{so} = \sqrt{\varepsilon_s X_{dep0} / C_{ox}}
\]

\[
l_2 = \sqrt{\varepsilon_s X_{dep} / C_{ox} \left( 1 + D_{VT2} V_{beff} \right)}
\]

\[
l_{rw} = \sqrt{\varepsilon_s X_{dep} / C_{ox} \left( 1 + D_{VT2w} V_{beff} \right)}
\]

\[
X_{dep} = \frac{2 \varepsilon_s \left( \Phi_s - V_{beff} \right)}{qN_{ch}}
\]

\[
X_{dep0} = \frac{2 \varepsilon_s \Phi_s}{qN_{ch}}
\]

\[
V_{beff} = V_{bc} + 0.5 \left[ V_{hs} - V_{bc} - \delta_i + \sqrt{(V_{hs} - V_{bc} - \delta_i)^2 - 4 \delta_i V_{bc}} \right]
\]

\[
\delta_i = 0.001 \text{V}
\]

\[
V_{bc} = 0.9 \left( \Phi_s - \frac{K_1^2}{4 K_2^2} \right)
\]

\[
V_{bi} = v_i \ln \left( \frac{N_{ch} N_{DS}}{n_i^2} \right)
\]
\[ N_{DS} = 1 \times 10^{20}/\text{cm}^3 \]

where \( T_{oxm} \) is the gate oxide thickness at which parameters are extracted with a default value of \( T_{ox} \).

### Threshold Voltage Model Parameters:

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>( TOX )</td>
<td>m</td>
<td>150e-10</td>
<td>Gate oxide thickness</td>
</tr>
<tr>
<td>( VTH0 )</td>
<td>V</td>
<td>0.7</td>
<td>Threshold voltage of long channel device at ( V_{bd}=0 ) and small ( V_{ds} ) (typically 0.7 for n-channel, -0.7 for p-channel)</td>
</tr>
<tr>
<td>( NSUB )</td>
<td>cm(^3)</td>
<td>6.0e16</td>
<td>Substrate doping concentration</td>
</tr>
<tr>
<td>( NCH )</td>
<td>cm(^3)</td>
<td>1.7e17</td>
<td>Peak doping concentration near interface</td>
</tr>
<tr>
<td>( NLX )</td>
<td>m</td>
<td>1.74e17</td>
<td>Lateral nonuniform doping along channel</td>
</tr>
<tr>
<td>( K1 )</td>
<td>V(^{1/2})</td>
<td>0.50</td>
<td>First-order body effect coefficient</td>
</tr>
<tr>
<td>( K2 )</td>
<td>-</td>
<td>-0.0186</td>
<td>Second-order body effect coefficient</td>
</tr>
<tr>
<td>( K3 )</td>
<td>-</td>
<td>80.0</td>
<td>Narrow width effect coefficient</td>
</tr>
<tr>
<td>( K3B )</td>
<td>1/V</td>
<td>0</td>
<td>Body width coefficient of narrow width effect</td>
</tr>
<tr>
<td>( W0 )</td>
<td>M</td>
<td>2.5e-6</td>
<td>Narrow width effect coefficient</td>
</tr>
<tr>
<td>( DVT0W )</td>
<td>1/m</td>
<td>0</td>
<td>Narrow width coefficient 0, for ( V_{th} ), at small ( L )</td>
</tr>
<tr>
<td>( DVT1W )</td>
<td>1/m</td>
<td>5.3e6</td>
<td>Narrow width coefficient 1, for ( V_{th} ), at small ( L )</td>
</tr>
<tr>
<td>( DVT2W )</td>
<td>1/V</td>
<td>-0.032</td>
<td>Narrow width coefficient 2, for ( V_{th} ), at small ( L )</td>
</tr>
<tr>
<td>( DVT0 )</td>
<td>-</td>
<td>2.2</td>
<td>Short channel effect coefficient 0, for ( V_{th} )</td>
</tr>
<tr>
<td>( DVT1 )</td>
<td>-</td>
<td>0.53</td>
<td>Short channel effect coefficient 1, for ( V_{th} )</td>
</tr>
<tr>
<td>( DVT2 )</td>
<td>1/V</td>
<td>-0.032</td>
<td>Short channel effect coefficient 2, for ( V_{th} )</td>
</tr>
<tr>
<td>( ETA0 )</td>
<td>-</td>
<td>0.08</td>
<td>Subthreshold region DIBL ( \text{(Drain Induced Barrier Lowering)} ) coefficient</td>
</tr>
<tr>
<td>( ETA1 )</td>
<td>1/V</td>
<td>-0.07</td>
<td>Subthreshold region DIBL coefficient</td>
</tr>
<tr>
<td>( DSUB )</td>
<td>-</td>
<td>DROUT</td>
<td>DIBL coefficient exponent in subthreshold region</td>
</tr>
<tr>
<td>( VBM )</td>
<td>V</td>
<td>-3.0</td>
<td>Maximum substrate bias, for ( V_{th} ) calculation</td>
</tr>
</tbody>
</table>

Other related model parameters: 13 parameter of \( L_{eff} \), \( W_{eff} \), and \( W_{eff} \).

### Effects on Threshold Voltage

1. **Short-Channel effect**
   
   \( L_{drawn} \downarrow \Rightarrow V_{th} \downarrow \).
   
   *Effective \( Q_{th} \) shared by source-drain junction depletion changes*

   **HSPICE Model Parameters:** \( DVT0, DVT1, DVT2 \)

2. **Narrow-Channel effect**
   
   \( W_{drawn} \downarrow \Rightarrow V_{th} \uparrow \).
   
   *Effective \( Q_{th} \) up by \( \Delta Q_{th} \) caused by the fringing electric field*

   ![Depletion region diagram](image)
HSPICE Model Parameters: K3, K3B, W0, DVT0W, DVT1W, DVT2W

3 DIBL (Drain-Induced Barrier Lowering) effect

\[ V_{DS} \uparrow \Rightarrow \text{electrons in the channel can be induced by the positive voltage at the drain as that at the gate} \]

\[ \Rightarrow V_{th} \downarrow \]

HSPICE Model Parameters: ETA0, ETAB, DSUB

4 Body effect

HSPICE Model Parameters: NLX, K1, K2, VBM

§ 1-1.3 First-Order MOS \( I_{DS} - V_{DS} \) Equations

**Linear, non-saturation, or triode region (\( V_{DS} < V_{DSAT}, V_{GS} > V_{TH} \))**

\[
I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W_{eff}}{L_{eff}} \left[ 2V_{DS} (V_{GS} - V_{TH}) - V_{DS}^2 \right]
\]

\( \mu_n \): electron surface mobility

\( L_{eff} = L_{drawn} - 2dL \)

\( W_{eff} = W_{drawn} - 2dW \)

\( V_{TH} = V_{THO} - \gamma (\sqrt{\Phi_S - V_{BS}} - \sqrt{\Phi_S}) \)

**Saturation region (\( V_{DS} > V_{DSAT}, V_{GS} > V_{TH} \))**

\[
I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{TH}) \left( 1 + \lambda V_{DS} \right)
\]

\( \lambda \): effective Early-Effect factor

\[
\lambda = \frac{1}{10} V^{-1} \text{ or } \frac{1}{100} V^{-1}
\]

\[
\lambda \approx \sqrt{\frac{2\varepsilon_{si}}{qN_{SUB}}} \frac{1}{2L \sqrt{V_{DS} - V_{DSAT}}}
\]
Saturation region or weak inversion region: \( V_{TH} - V_{eff} < V_{GS} < V_{TH} \)

\[
I_{DS} \equiv I_{so} \exp\left(\frac{V_{GS}}{nV_t}\right) \left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right]
\]

\[
I_{so} = \mu_{0} \frac{W_{eff}}{L_{eff}} \sqrt{\frac{q \varepsilon_{si} N_{ch}}{2 \Phi_s}} V_t^2
\]

\[
n \geq 1 + \frac{C_d}{C_{ox}} = 1 + \frac{1}{C_{ox}} \sqrt{\frac{2 \Phi_{s} - V_{DS}}{q \varepsilon_{si} N_{ch}}}
\]

1-1.4 Level 49 BSIM3 Version 3 SPICE MOS Model – \( I_{DS} - V_{DS} \) Equation

1. Effective \( (V_{GS} - V_{TH}) = V_{GST} \)

\[
V_{gst} = \frac{2 n V_t \ln \left[1 + \exp\left(\frac{V_{gst} - V_{th}}{2 n V_t}\right)\right]}{1 + 2 n C_{ox} \sqrt{\frac{2 \Phi_s}{q \varepsilon_{si} N_{ch}}} \exp\left(-\frac{V_{gst} - V_{th} - 2 V_{eff}}{2 n V_t}\right)}
\]

\[
n = 1 + N_{factor} \frac{C_d}{C_{ox}} + \left(\frac{C_{ds} + C_{dscl} V_{ds} + C_{dsclb} V_{b eff}}{C_{ox}} \exp\left(-D_{VTI} \frac{L_{eff}}{l_t}\right) + 2 \exp\left(-D_{VTI} \frac{L_{eff}}{l_t}\right)\right) + \frac{C_{ff}}{C_{ox}}
\]

\[
C_d = \frac{\varepsilon_{si}}{X_{dep}}
\]

Effective \( (V_{GS} - V_{TH}) \) Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOFF</td>
<td>V</td>
<td>-0.08</td>
<td>Offset voltage in subthreshold region</td>
</tr>
<tr>
<td>NFACCTOR</td>
<td>-</td>
<td>1.0</td>
<td>Subthreshold region swing</td>
</tr>
<tr>
<td>CIT</td>
<td>F/m²</td>
<td>0.0</td>
<td>Interface state capacitance</td>
</tr>
<tr>
<td>CDSC</td>
<td>F/m²</td>
<td>2.4e-4</td>
<td>Drain/source and channel coupling capacitance</td>
</tr>
<tr>
<td>CDSCD</td>
<td>F/\text{Vm}²</td>
<td>0</td>
<td>Drain bias sensitivity of CDSC</td>
</tr>
<tr>
<td>CDSCB</td>
<td>F/\text{Vm}²</td>
<td>0</td>
<td>Body coefficient for CDSC</td>
</tr>
</tbody>
</table>

Other related model parameters: 20 parameters of \( V_{th} \), and 13 parameters of \( L_{eff} \), \( W_{eff} \), and \( W_{eff}' \).

2. Mobility

For \( \text{mobMod}=1 \) (Default)

\[
\mu_{eff} = \frac{\mu_{0}}{1 + \left(U_{a} + U_{c} V_{b eff} \left(\frac{V_{gst} + 2 V_{th}}{T_{ox}}\right) + U_{a} \left(\frac{V_{gst} + 2 V_{th}}{T_{ox}}\right)^2\right)}
\]
Mobility Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
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<th>Comments</th>
</tr>
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<tbody>
<tr>
<td>U0</td>
<td>cm²/V·sec</td>
<td>670 nms</td>
<td>Low field mobility at T=TREF=TNOM</td>
</tr>
<tr>
<td>Ua</td>
<td>m/V</td>
<td>2.25e-9</td>
<td>First-order mobility degradation coefficient</td>
</tr>
<tr>
<td>Ub</td>
<td>m²/V²</td>
<td>5.87e-19</td>
<td>Second-order mobility degradation coefficient</td>
</tr>
<tr>
<td>Uc</td>
<td>1/V</td>
<td>-4.65e-11 or -0.0465</td>
<td>Body bias sensitivity coefficient of mobility</td>
</tr>
</tbody>
</table>

Other related model parameters: 20 parameters of \( V_{th} \), 6 parameters of \( V_{gstr} \), and 13 parameters of \( L_{eff} \), \( W_{eff} \), and \( W_{eff}' \)

3. Drain Saturation Voltage

For \( R_{ds} > 0 \) or \( \lambda \neq 1 \):

\[
V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}
\]

\[
a = A_{bulk}^2 W_{eff} V_{sat} C_{ox} R_{DS} + \left( \frac{1}{\lambda} - 1 \right) A_{bulk}
\]

\[
b = -\left( V_{gstr} + 2V_t \left( \frac{2}{\lambda} - 1 \right) + A_{bulk} E_{sat} L_{eff} + 3A_{bulk} \left( V_{gstr} + 2V_t \right) W_{eff} V_{sat} C_{ox} R_{DS} \right)
\]

\[
c = \left( V_{gstr} + 2V_t \right) E_{sat} L_{eff} + 2 \left( V_{gstr} + 2V_t \right) W_{eff} V_{sat} C_{ox} R_{DS}
\]

\[
\lambda = A_{g} V_{gstr} + A_{2}
\]

For \( R_{DS} = 0 \) and \( \lambda = 1 \)

\[
V_{dsat} = \frac{E_{sat} L_{eff} \left( V_{gstr} + 2V_t \right)}{A_{bulk} E_{sat} L_{eff} + \left( V_{gstr} + 2V_t \right)}
\]

\[
A_{bulk} = \left[ 1 + \frac{K_{hox}}{2V_{bsseff}} \right] \left[ \frac{A_{0} L_{eff}}{L_{eff} + 2 \sqrt{X_{j} X_{dep}}} \right] \left[ 1 - A_{g} V_{gstr} \left[ \frac{L_{eff}}{L_{eff} + 2 \sqrt{X_{j} X_{dep}}} \right]^2 + \frac{B_{0}}{W_{eff}} \right] + \frac{1}{1 + K_{e} V_{bsseff}}
\]

\[
E_{sat} = \frac{2V_{sat}}{\mu_{eff}}
\]
Drain Saturation Voltage Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>-</td>
<td>1.0</td>
<td>Bulk charge effect coefficient for channel length</td>
</tr>
<tr>
<td>AGS</td>
<td>1/V</td>
<td>0.0</td>
<td>Gate bias coefficient of Abulk</td>
</tr>
<tr>
<td>B0</td>
<td>m</td>
<td>0.0</td>
<td>Bulk charge effect coefficient for channel</td>
</tr>
<tr>
<td>B1</td>
<td>m</td>
<td>0.0</td>
<td>Bulk charge effect width offset</td>
</tr>
<tr>
<td>KETA</td>
<td>1/V</td>
<td>-0.047</td>
<td>Body-bias coefficient of bulk charge effect</td>
</tr>
<tr>
<td>VSAT</td>
<td>msec</td>
<td>8e4</td>
<td>Saturation velocity of carrier at T=TREF=Tnom</td>
</tr>
<tr>
<td>A1</td>
<td>1/V</td>
<td>0</td>
<td>First nonsaturation factor</td>
</tr>
<tr>
<td>A2</td>
<td>-</td>
<td>1.0</td>
<td>Second nonsaturation factor</td>
</tr>
<tr>
<td>XJ</td>
<td>m</td>
<td>0.15e-6</td>
<td>Junction depth</td>
</tr>
</tbody>
</table>

Other related model parameters: 20 Vth, 6Vgsteff, 13 Leff, Weff, and Weff', and 4RDS

4. Effective V_DS

\[ V_{d_{eff}} = V_{dsat} - \frac{1}{2} \left( V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}} \right) \]

Effective V_DS Model Parameter

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELTA</td>
<td>V</td>
<td>0.01</td>
<td>Effective Vds parameter</td>
</tr>
</tbody>
</table>

Other related model parameters: 9Vsat, 20 Vth, 6Vgsteff, 13 Leff, Weff, and Weff', and 4RDS

5. Drain Current Expression

\[ I_{ds} = \frac{I_{d_{o}(v_{steff})}}{1 + \frac{R_{ds} I_{d_{o}(v_{steff})}}{V_{d_{eff}}}} \left( 1 + \frac{V_{ds} - V_{d_{eff}}}{V_A} \right) \left( 1 + \frac{V_{ds} - V_{d_{eff}}}{V_{ASCBE}} \right) \]

\[ I_{d_{o}} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gsteff}}{L_{eff} \left[ 1 + V_{d_{eff}} \left( \frac{E_{sat}}{L_{eff}} \right) \right]} \left( 1 - \frac{V_{d_{eff}}}{2(V_{gsteff} + 2V_{t})} \right) \]

\[ V_A = V_{sat} \left[ 1 + \frac{P_{v_{seff}} V_{gsteff}}{E_{sat} L_{eff}} \left( \frac{1}{V_{ACLM}} + \frac{1}{V_{ADBLC}} \right)^{-1} \right] \]

\[ V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat} L_{eff}} (V_{ds} - V_{d_{eff}}) \]

\[ V_{ADBLC} = \frac{V_{gsteff} + 2V_{t}}{\theta_{rot} \left( \left( 1 + P_{DIBL2} V_{steff} \right) \left( 1 - A_{bulk} V_{dsat} + V_{gsteff} + 2V_{t} \right) \right)} \]

\[ \theta_{rot} = P_{DIBL1C} \left[ \exp \left( -D_{ROUT} \frac{L_{eff}}{2l_{0}} \right) + 2 \exp \left( -D_{ROUT} \frac{L_{eff}}{l_{0}} \right) \right] + P_{DIBL2} \]

\[ \frac{1}{V_{ASCBE}} = \frac{P_{spe2}}{L_{eff}} \exp \left( -P_{spe2} \frac{V_{ds}}{V_{d_{eff}}} \right) \]
\[
V_{\text{Sat}} = \frac{E_{\text{sat}} L_{\text{eff}} + V_{\text{dut}} + 2R_D V_{\text{sat}} C_{\text{ox}} W_{\text{eff}} V_{\text{geff}}}{2/\lambda - 1} \left( 1 - \frac{A_{\text{bulk}} V_{\text{dut}}}{2(V_{\text{geff}} + 2V_f)} \right)
\]

\[
litl = \sqrt{\frac{\varepsilon_{\text{sat}} T_{\text{ox}} X_f}{\varepsilon_{\text{ox}}}}
\]

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCLM</td>
<td>-</td>
<td>1.3</td>
<td>Coefficient of channel length modulation values ( \leq 0 ) will result in an error message and program exit</td>
</tr>
<tr>
<td>PDIBLC1</td>
<td>-</td>
<td>0.39</td>
<td>DIBL (Drain Induced Barrier Lowering) Effect coefficient 1</td>
</tr>
<tr>
<td>PDIBLC2</td>
<td>-</td>
<td>0.0086</td>
<td>DIBL effect coefficient 2</td>
</tr>
<tr>
<td>PDIBLCB</td>
<td>1/V</td>
<td>0</td>
<td>Body effect coefficient of DIBL effect coefficients</td>
</tr>
<tr>
<td>DROUT</td>
<td>-</td>
<td>0.56</td>
<td>Length dependence coefficient of the DIBL Correction parameter in Rout</td>
</tr>
<tr>
<td>PVAG</td>
<td>-</td>
<td>0</td>
<td>Gate dependence of Early voltage</td>
</tr>
</tbody>
</table>

Other related model parameters: 1\( V_{\text{dut}} \), 9\( V_{\text{sat}} \), 20\( V_{\text{th}} \), 6\( V_{\text{geff}} \), 13\( L_{\text{eff}} \), \( W_{\text{eff}} \), and \( 4R_{\text{DS}} \).

6. Substrate Current

\[
I_{\text{sub}} = \alpha_0 (V_d - V_{\text{dut}}) \exp\left( -\frac{\beta_0}{V_d - V_{\text{dut}}} \right) \left[ \frac{I_{\text{ds}}}{1 + \frac{V_{\text{ds}} - V_{\text{dut}}}{V_A}} \right]
\]

Substrate Current Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALPHAO0</td>
<td>m/V</td>
<td>0</td>
<td>The first parameter of impact ionization current</td>
</tr>
<tr>
<td>BETA0</td>
<td>V</td>
<td>30</td>
<td>The second parameter of impact ionization current</td>
</tr>
</tbody>
</table>

Other related model parameters: 1\( V_{\text{dut}} \), 9\( V_{\text{sat}} \), 20\( V_{\text{th}} \), 6\( V_{\text{geff}} \), 13\( L_{\text{eff}} \), \( W_{\text{eff}} \), and \( 4R_{\text{DS}} \).

7. Subthreshold Drain Current

\[
I_d = I_o (1 - \exp(-\frac{V_d}{V_t})) \exp\left( \frac{V_{\text{geff}} + |V_{\text{off}}|}{nV_t} \right)
\]

\[
I_o = \mu_0 \frac{W_{\text{eff}}}{L_{\text{eff}}} \sqrt{\frac{q \varepsilon_{\text{Si}} N_{\text{ch}}}{2\Phi_s}} V_t^2
\]

where \( V_{\text{off}} \) is the offset voltage which is an important parameters determining the drain current at \( V_{gs} = 0 \).
8. Polysilicon Depletion Effect

\[ V_{\text{poly}} = \frac{1}{2} x_{\text{poly}} E_{\text{poly}} = \frac{q N_{\text{gate}} X_{\text{poly}}^2}{2 \varepsilon_{\text{i}}^2} \]

\[ \varepsilon_{\text{ox}} E_{\text{ox}} = \varepsilon_{\text{si}} E_{\text{poly}} = \sqrt{2 q \varepsilon_{\text{i}} N_{\text{gate}} V_{\text{poly}}} \]

\[ V_{\text{gs}} - V_{\text{FB}} - \Phi_{s} = V_{\text{poly}} + V_{\text{ox}} \]

\[ a(V_{\text{gs}} - V_{\text{FB}} - \Phi_{s} - V_{\text{poly}})^2 - V_{\text{poly}} = 0 \]

\[ a = \frac{\varepsilon_{\text{ox}}^2}{2 q \varepsilon_{\text{i}} N_{\text{gate}} T_{\text{ox}}^2} \]

\[ V_{\text{gs, eff}} = V_{\text{FB}} + \Phi_{s} + \frac{2 q \varepsilon_{\text{i}} N_{\text{gate}}}{\varepsilon_{\text{ox}}^2} T_{\text{ox}}^2 \left( \sqrt{1 + \frac{2 \varepsilon_{\text{i}}}{q \varepsilon_{\text{i}} N_{\text{gate}} T_{\text{ox}}^2} (V_{\text{gs}} - V_{\text{FB}} - \Phi_{s}) - 1} \right) \]

Polysilicon Depletion Effect Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>NGATE</td>
<td>cm(^3)</td>
<td>infinite</td>
<td>Poly gate doping concentration</td>
</tr>
</tbody>
</table>

9. Effective Channel Length and Width

\[ L_{\text{eff}} = L_{\text{drawn}} - 2dL \]

\[ W_{\text{eff}} = W_{\text{drawn}} - 2dw \]

\[ W_{\text{eff}} = W_{\text{drawn}} - 2dW' \]

\[ dW = dW' + dW_{g} V_{\text{g}} + dW_{b} \left( \Phi_{s} - V_{\text{beff}} - \sqrt{\Phi_{s}} \right) \]

\[ dW' = W_{t} + \frac{W_{l}}{L_{\text{in}}} + \frac{W_{w}}{L_{\text{un}}} + \frac{W_{sd}}{L_{\text{un}} W_{\text{un}}} \]

\[ L_{\text{eff}} = L_{\text{drawn}} - 2dL \]

\[ dL = L_{\text{int}} + \frac{L_{d}}{L_{\text{in}}} + \frac{L_{o}}{W_{\text{un}}} + \frac{L_{n}}{L_{\text{un}} W_{\text{un}}} \]

Effective Channel Length and Width Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>WINT</td>
<td>m</td>
<td>0.0</td>
<td>Width offset fitting parameter from I-V without bias</td>
</tr>
<tr>
<td>WLN</td>
<td>-</td>
<td>1.0</td>
<td>Power of length dependence of width offset</td>
</tr>
<tr>
<td>WW</td>
<td>m(^{\text{WLN}})</td>
<td>0.0</td>
<td>Coefficient of width dependence fo width</td>
</tr>
</tbody>
</table>
Other related model parameters: $6V_{g_{st}}$ and $20V_{th}$

10. Source/Drain Resistance

![Source/Drain Resistance Equation]

### Source/Drain Resistance Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DSW}$</td>
<td>ohm · μm</td>
<td>0.0</td>
<td>Parasitic source drain resistance per unit width</td>
</tr>
<tr>
<td>$PRWG$</td>
<td>1/V</td>
<td>0</td>
<td>Gate bias effect coefficient of $R_{DSW}$</td>
</tr>
<tr>
<td>$PRWB$</td>
<td>1/V$^{1/2}$</td>
<td>0</td>
<td>Body effect coefficient of $R_{DSW}$</td>
</tr>
<tr>
<td>$WR$</td>
<td>-</td>
<td>1.0</td>
<td>Width offset from $W_{eff}$ for $R_{ds}$ calculation</td>
</tr>
</tbody>
</table>

11. Temperature Effects

$$V_{ds(T)} = V_{ds(T_{norm})} + \left( K_1 + K_2 / L_{ds} + K_3 V_{ds(T_{norm})} \right) (T / T_{norm} - 1)$$

$$\mu(T) = \mu(T_{norm}) \left( \frac{T}{T_{norm}} \right)^{1/2}$$

$$V_{sat(T)} = V_{sat(T_{norm})} - A_r (T / T_{norm} - 1)$$

$$R_{ds(T)} = R_{ds(T_{norm})} + P_{r} \left( \frac{T}{T_{norm}} - 1 \right)$$

$$U_{rl(T)} = U_{rl(T_{norm})} + U_{rl}(T / T_{norm} - 1)$$

$$U_{dt(T)} = U_{dt(T_{norm})} + U_{dt}(T / T_{norm} - 1)$$

$$U_{ct(T)} = U_{ct(T_{norm})} + U_{ct}(T / T_{norm} - 1)$$
Temperature Effects Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>KT1</td>
<td>V</td>
<td>0.0</td>
<td>Temperature coefficient for Vth</td>
</tr>
<tr>
<td>KTIL</td>
<td>m-V</td>
<td>0.0</td>
<td>Temperature coeff. for channel length dependence of Vth</td>
</tr>
<tr>
<td>KT2</td>
<td>-</td>
<td>0.022</td>
<td>Body bias coefficient of Vth temperature effect</td>
</tr>
<tr>
<td>UTE</td>
<td>-</td>
<td>-1.5</td>
<td>Mobility temperature exponent</td>
</tr>
<tr>
<td>UA1</td>
<td>m/V</td>
<td>4.31e-9</td>
<td>Temperature coefficient for UA</td>
</tr>
<tr>
<td>UBI</td>
<td>(m/V)^2</td>
<td>-7.61e-18</td>
<td>Temperature coefficient for UB</td>
</tr>
<tr>
<td>UCI</td>
<td>m/V^2</td>
<td>-5.69e-11</td>
<td>Temperature coefficient for UC</td>
</tr>
<tr>
<td>AT</td>
<td>m/sec</td>
<td>3.3e4</td>
<td>Temperature coefficient for saturation velocity</td>
</tr>
<tr>
<td>PRT</td>
<td>ohm-um</td>
<td>0</td>
<td>Temperature coefficient for RDSW</td>
</tr>
</tbody>
</table>

1-1.5 Level 49 BSIM3 Version 3 SPICE MOS Model-MOS Diode Equations

1. I-V model of S/B diode

   \[
   i_{th} \neq 0 \\
   \text{If } V_{bs} < V_{jim} \\
   I_{bs} = I_{th} \left[ \exp \left( \frac{V_{bs}}{N \nu_t} \right) - 1 \right] + G_{min} V_{bs} \\
   \text{otherwise} \\
   I_{bs} = i_{th} + \frac{i_{th} + I_{th}}{N \nu_t} (V_{bs} - V_{jim}) + G_{min} V_{bs} \\
   V_{jim} = N \nu_t \ln \left( \frac{i_{th}}{I_{th}} + 1 \right) \\
   I_{bs} = A_{S_{eff}} J_s + P_{S_{eff}} J_{SW} \\
   A_{S_{eff}} = 2 \cdot HDIF \cdot SCALM \cdot WMLT \cdot W_{eff} \text{ (As is not specified)} \\
   A_{S_{eff}} = M \cdot A_S \cdot WMLT^2 \cdot SCALE^2 \text{ (As is specified)} \\
   P_{S_{eff}} = 4 \cdot HDIF \cdot SCALM \cdot WMLT \text{ (Ps is not specified)} \\
   P_{S_{eff}} = M \cdot P_S \cdot SCALE \cdot WMLT \\
   A_{S_{eff}} : \text{ effective source junction area} \\
   \]
\( P_{S_{of}} \): effective source junction perimeter

\( \text{SCALE (SCALM)} \): scaling for element (model) statement parameters

Temperature effect

\[
J_S(T) = J_S(T_{\text{nom}}) \exp \left[ \frac{E_{g_0} - E_g}{v_{l0} - v_l} + XT I \cdot \ln \left( \frac{T}{T_{\text{nom}}} \right) \right] \frac{N}{N_{\text{nom}}}
\]

\[
J_{SW}(T) = J_{SW}(T_{\text{nom}}) \exp \left[ \frac{E_{g_0} - E_g}{v_{l0} - v_l} + XT I \cdot \ln \left( \frac{T}{T_{\text{nom}}} \right) \right] \frac{N}{N_{\text{nom}}}
\]

\[
E_{g_0} = 1.16 - \frac{7.02 \times 10^{-4} T_{\text{nom}}^2}{T_{\text{nom}} + 1108}
\]

\[
E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}
\]

2. I-V model of D/B diode

\( V_{bs} \rightarrow V_{bd} \)

\( V_{jm} \rightarrow V_{jdm} \)

\( I_{bs} \rightarrow I_{bsd} \)

\( A_{s} \rightarrow A_{d} \)

\( P_{s} \rightarrow P_{d} \)

MOS Diode I-V model parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>( JS )</td>
<td>A/m²</td>
<td>0.0</td>
<td>Bulk junction saturation current (Default deviates from BSIM3v3=1.0e⁻⁴)</td>
</tr>
<tr>
<td>( JSW )</td>
<td>A/m</td>
<td>0.0</td>
<td>Sidewall bulk junction saturation current</td>
</tr>
<tr>
<td>( NJ )</td>
<td>-</td>
<td>1</td>
<td>Emission coefficient (not used with ACM=3)</td>
</tr>
<tr>
<td>( XT I )</td>
<td>-</td>
<td>3.0</td>
<td>Junction current temperature exponent</td>
</tr>
</tbody>
</table>

MOS Geometry Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Unit</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( HDIF )</td>
<td>m</td>
<td>0</td>
<td>Length of heavily doped diffusion, from contact to lightly doped region (ACM=2,3 only)</td>
</tr>
</tbody>
</table>
**LD**  m  Lateral diffusion into channel from source and drain diffusion.

If LD and XJ are unspecified, LD default=0.0.

When LD is unspecified, but XJ is specified, LD is calculated from XJ. LD default=0.75 \times XJ.

For Level 4 only, lateral diffusion is derived from LD \times XJ.

LD_{scaled} = LD \times SCALM

**LDIF**  m  0  Length of lightly doped diffusion adjacent to gate (ACM=1,2)

LDIF_{scaled} = LDIF \times SCALM

**WMLT**  1  Width diffusion layer shrink reduction factor

§ 1-2 Small-Signal Model of MOSFETs

\[ G \quad C_{gd} \quad C_{gb} \quad C_{gs} \quad g_{m} V_{gs} \quad g_{mb} V_{bs} \quad g_{ds} \quad R_{S} \quad C_{bs} \quad C_{bd} \quad R_{D} \quad D \]

\[ G \quad S \quad B \]

As=W \cdot Is  bottom plate source junction area

Ad=W \cdot Id  bottom plate drain junction area

Ps=2(W+Is)  perimeter of source junction

Pd=2(W+Id)  perimeter of drain junction
\[ C_{\text{gsov}}(C_{\text{gdov}}) = C_o \cdot L_D = \text{CGSO(CGDO)} \]

\[ C_{\text{jsb}} = C_{\text{j}} A_s \left( \frac{1}{1 - \frac{V_{\text{BS}}}{P_{\text{f}}} \cdot \text{MJ}} + C_{\text{jw}} P_s \frac{1}{1 - \frac{V_{\text{BS}}}{P_{\text{f}}} \cdot \text{MJSW}} \right) \]

\[ V_{\text{BS}}^+: \text{forward bias; } - V_{\text{BS}}^-:\text{reverse bias} \]

\[ C_{\text{sem}} = \frac{\varepsilon_{\text{si}} \cdot x_d}{\varepsilon_{\text{si}}} = \frac{1}{2} \varepsilon_{\text{si}} \frac{Q_s - V_{\text{BS}}}{q N_A} (N_D) \]

\[ g_m = \frac{\partial I_{\text{DS}}}{\partial V_{\text{GS}}} = \frac{2}{\sqrt{I_{\text{DS}}}} \frac{\mu_n C_o W}{2 L} \text{ (sat. region)} \]

\[ g_{\text{mb}} = \frac{\partial I_{\text{DS}}}{\partial V_{\text{BS}}} = \frac{\text{GAMMA } g_m}{2 \sqrt{Q_s - V_{\text{BS}}}} = g_m \eta \text{ (sat. region)} \]

\[ \eta = \frac{\text{GAMMA}}{2 \sqrt{Q_s - V_{\text{BS}}} \text{ (sat.)} \quad R_{\text{D}}, R_{\text{S}}: \text{drain/source resistance} \]

\[ \frac{1}{r_{\text{ds}}} = g_{\text{ds}} = \frac{\partial I_{\text{DS}}}{\partial V_{\text{DS}}} \equiv \lambda I_D \text{ (sat.)} \quad R_{\text{D}}, R_{\text{S}}: \text{drain/source resistance} \]

**Table: OFF, LINEAR, SATURATION**

| \( \) | OFF \hspace{1cm} \text{LINEAR} \hspace{1cm} \text{SATURATION} \ |
|---|---|---|
| \( C_{\text{gs}} \) | \( C_{\text{gsov}} W \) | \( WC_{\text{gsov}} + \frac{1}{2} C_o W L \) | \( WC_{\text{gsov}} + \frac{2}{3} C_o W L \) |
| \( C_{\text{gd}} \) | \( C_{\text{gdov}} W \) | \( WC_{\text{gdov}} + \frac{1}{2} C_o W L \) | \( WC_{\text{gdov}} \) |
| \( C_{\text{gb}} \) | \( 0.9C_o W L \) | 0 | 0.1C_o W L |
| \( C_{\text{bs}} \) | \( C_{\text{jsb}} \) | \( C_{\text{jsb}} + \frac{1}{2} C_{\text{sem}} W L \) | \( C_{\text{jsb}} + \frac{2}{3} C_{\text{sem}} W L \) |
| \( C_{\text{bd}} \) | \( C_{\text{jbd}} \) | \( C_{\text{jbd}} + \frac{1}{2} C_{\text{sem}} W L \) | \( C_{\text{jbd}} \) |

Exact calculation of \( C_{\text{gs}} \cdot C_{\text{gd}} \) and \( C_{\text{gb}} \):
Typical device
Transconductance (gm) versus drain current (I_d)

gm for BJT > gm for MOS

Parameter $\eta = \frac{\text{GAMMA}}{2\sqrt{\Phi_s} - V_{BS}}$ versus $|V_{BS}|$

✧ In this figure, $|V_{BS}| = 0 \ V$ does not mean short-circuited substrate and source!

Junction Capacitance Model Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACM</td>
<td>-</td>
<td>0</td>
<td>Area calculation method selector (Start-Hspice specific)</td>
</tr>
<tr>
<td>CJ</td>
<td>F/m²</td>
<td>5.79e-4</td>
<td>zero-bias bulk junction capacitance (Default deviates from BSIM3v3 = 5.0e-4)</td>
</tr>
<tr>
<td>CJSW</td>
<td>F/m</td>
<td>0.0</td>
<td>zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3v3 = 5.0e-10)</td>
</tr>
<tr>
<td>Name</td>
<td>Units</td>
<td>Default</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>-------</td>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>CJSWG</td>
<td>F/m</td>
<td>CJSW</td>
<td>zero-bias gate-edge sidewall bulk junction capacitance (not used with ACM=0-3)</td>
</tr>
<tr>
<td>PB</td>
<td>V</td>
<td>1.0</td>
<td>bulk junction contact potential</td>
</tr>
<tr>
<td>PBSW</td>
<td>V</td>
<td>1.0</td>
<td>sidewall bulk junction contact potential</td>
</tr>
<tr>
<td>MJ</td>
<td>-</td>
<td>0.5</td>
<td>bulk junction grading coefficient</td>
</tr>
<tr>
<td>MJSW</td>
<td>-</td>
<td>0.33</td>
<td>sidewall bulk junction grading coefficient</td>
</tr>
<tr>
<td>PHP</td>
<td>V</td>
<td>PB</td>
<td>bulk sidewall junction contact potential</td>
</tr>
</tbody>
</table>

Note that ACM=2 (UMC 0.5μm CMOS) invokes the standard Start-Hspice junction model in pg. 15-40 to 15-51, Start-Hspice Manual, Release 1998.2.


**Junction Resistance Model Parameters**

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD</td>
<td>ohm/sq</td>
<td>0.0</td>
<td>drain ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.</td>
</tr>
<tr>
<td>RDC</td>
<td>ohm</td>
<td>0.0</td>
<td>additional drain resistance due to contact resistance</td>
</tr>
<tr>
<td>RS</td>
<td>ohm/sq</td>
<td>0.0</td>
<td>source ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.</td>
</tr>
<tr>
<td>RSC</td>
<td>ohm</td>
<td>0.0</td>
<td>additional source resistance due to contact resistance</td>
</tr>
<tr>
<td>RSH</td>
<td>ohm/sq</td>
<td>0.0</td>
<td>drain and source diffusion sheet resistance</td>
</tr>
</tbody>
</table>

**AC and capacitance model parameter**

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAPMOD</td>
<td>-</td>
<td>0</td>
<td>Selects from BSIM3 versions 3.0 3.1 3.11(version=3.11 is the HSPICE97.4 equivalent to BSIM3v3 version3.1)</td>
</tr>
<tr>
<td>XPART</td>
<td>-</td>
<td>1</td>
<td>Charge portioning rate flag(default deviates from BSIM3V3=0)</td>
</tr>
<tr>
<td>CGSO</td>
<td>F/m</td>
<td>P1(see Note1)</td>
<td>Non-LDD region source-gate overlap capacitance per unit channel length</td>
</tr>
</tbody>
</table>

Note 1: See the documentation for more details.
<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGDO</td>
<td>F/m</td>
<td>P2(see Note2)</td>
<td>Non-LDD region source-gate overlap capacitance per unit channel length</td>
</tr>
<tr>
<td>CGBO</td>
<td>F/m</td>
<td>0</td>
<td>Gate-bulk overlap capacitance per unit channel length</td>
</tr>
<tr>
<td>CGSI</td>
<td>F/m</td>
<td>0.0</td>
<td>Lightly doped source-gate overlap region capacitance</td>
</tr>
<tr>
<td>CGDI</td>
<td>F/m</td>
<td>0.0</td>
<td>Lightly doped source-gate overlap region capacitance</td>
</tr>
<tr>
<td>CKAPPA</td>
<td>F/m</td>
<td>0.6</td>
<td>Coefficient for lightly doped region overlap capacitance fringing field capacitance</td>
</tr>
<tr>
<td>CF</td>
<td>F/m</td>
<td>(see note3)</td>
<td>Fringing field capacitance</td>
</tr>
<tr>
<td>CLC</td>
<td>M</td>
<td>0.1e-6</td>
<td>Constant term for the short channel model</td>
</tr>
<tr>
<td>CLE</td>
<td>-</td>
<td>0.6</td>
<td>Exponential term for the short channel model</td>
</tr>
<tr>
<td>DLC</td>
<td>M</td>
<td>LINT</td>
<td>Length offset fitting parameter from CV</td>
</tr>
<tr>
<td>DWC</td>
<td>M</td>
<td>WINT</td>
<td>Width offset fitting parameter from CV</td>
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</table>

The capacitance model equation can be seen from BSIM 3v3.2.2 manual in appendix B. Note that capmod=2 and XPART=0 (0/100 charge partition)

§ 1-3 Other HSPICE Model parameter

Model Flags

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<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comment</th>
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</thead>
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<tr>
<td>VERSION</td>
<td>-</td>
<td>3.11</td>
<td>Selects from BSIM3 version 3.0,3.1,3.11 (version=3.11 is the HSPICE97.4 equivalent to BSIM3v3 version3.1)</td>
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<tr>
<td>BINFLAG</td>
<td>-</td>
<td>0</td>
<td>Uses wref, lref when set&gt;0.9</td>
</tr>
<tr>
<td>NOIMOD</td>
<td>-</td>
<td>1</td>
<td>Berkeley noise modelflag</td>
</tr>
<tr>
<td>NLEV</td>
<td>-</td>
<td>0(off)</td>
<td>Star-Hspice noise model flag (non-zero overrides NOIMOD)(star-HSPICE specific)</td>
</tr>
<tr>
<td>NQSMOD</td>
<td>-</td>
<td>0(off)</td>
<td>NQS Model is not supported in Level49</td>
</tr>
<tr>
<td>SFVTHFLA G</td>
<td>-</td>
<td>1(on)</td>
<td>Spline function for Vth(star-Hspice specific)</td>
</tr>
<tr>
<td>VFBFLAG</td>
<td>-</td>
<td>0(off)</td>
<td>UFB selector for CAPMOD=0(star-HSPICE specific)</td>
</tr>
</tbody>
</table>

Bin Description Parameter

<table>
<thead>
<tr>
<th>Name</th>
<th>Units</th>
<th>Default</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMIN</td>
<td>M</td>
<td>0.0</td>
<td>minimum channel length</td>
</tr>
<tr>
<td>LMAX</td>
<td>M</td>
<td>1.0</td>
<td>Maximum channel length</td>
</tr>
<tr>
<td>WMIN</td>
<td>M</td>
<td>0.0</td>
<td>minimum channel width</td>
</tr>
<tr>
<td>WMAX</td>
<td>M</td>
<td>1.0</td>
<td>Maximum channel width</td>
</tr>
<tr>
<td>BINUNIT</td>
<td>-</td>
<td>0</td>
<td>Flicker noise parameter</td>
</tr>
</tbody>
</table>

Process Parameter 5
Noise Parameter 7
NQS Parameter 1
Chapter 2  CMOS Process Technology and Layout

Rule

§ 2 – 1 Typical Submicron CMOS Process Flow

0.5μm SPDM twin-well polycide-gate CMOS technology

Major Process Steps:

1. Lightly-doped (15-20 Ω-cm , P) p-type substrate , <100>
2. N-well region definition (NW , Mask # 1)
3. N-well implantation (phosphorus)  Fig. 3-1

4. P-well region definition (PW , Mask # 2)
5. P-well implantation (Boron)  Fig. 3-2

---

Fig. 3-1
6. Well drive-in with 350 Å oxide growth, 1100°C
7. Oxide strip.
8. Pad oxide growth (200 Å) ±25 Å, 920°C
9. Si$_3$N$_4$ deposition (1500 Å) ±200 Å, 780°C
10. Field oxide definition (SN, Mask #3)
11. Si$_3$N$_4$ and pad oxide etch
12. Field oxidation (500 Å), 980°C
13. P-field implantation definition (PF, Mask #4)
14. P-field implantation (Boron) Fig. 3-3
15. Photoresist strip
16. Si$_3$N$_4$ and pad oxide removal
17. Pregate oxide growth (250 Å) and etch away
18. Pregate oxide growth (110 Å)
19. Threshold adjustment implantation (Boron) Fig. 3-4

Blanket threshold adjustment implantation

![Blanket threshold adjustment implantation diagram]

Fig. 3-4

20. Pregate oxide etching
21. Gate oxide growth (85 Å)
22. Polysilicon deposition (1500 Å)
23. Polysilicon doped with phosphorus (43 Ω/□)
24. WSi₂ deposition (1250 Å)
25. Polysilicon definition (PO, Mask #5)
26. Polysilicon etch Fig. 3-5

![Polysilicon definition diagram]

Fig. 3-5

27. NLDD implant definition (NM, Mask #6)
28. NLDD implantation (phosphorus and Asenic shallow implant)
29. WSi₂ anneal (180 Å)
30. PLDD implant definition (PM, Mask #7)
31. PLDD implantation (BF$_2$ shallow implant)  Fig. 3-6

![Diagram of PLDD implantation]

32. Conformal sidewall spacer oxide deposition (2000 Å), 700 °C
33. Anisotropic sidewall oxide etchback to form spacers
34. N$^+$ source/drain implant definition (NP, Mask #8)
35. N$^+$ source/drain implantation (As)  Fig. 3-7

![Diagram of N$^+$ source/drain implantation]

36. P$^+$ source/drain implant definition (PP, Mask #9)
37. P$^+$ source/drain implantation (BF$_2$)
38. Low Temperature Oxide (LTO) – Boron – Phosphate Silicon Glass (BPSG) deposition (9000 Å doped, 2000 Å undoped)
39. Flow, 850 °C
40. Contact definition (CO, Mask #10)
41. Contact etching
42. Annealing  
43. Plug barrier deposition (Ti 400 Å / TiN 1000 Å)
44. Barrier annealing
45. W Plug deposition 6000 Å
46. Metal 1 sputtering (AlCu 4000 Å / TiN 1400 Å)
47. Metal 1 definition (M1, Mask #11)
48. Metal 1 etching
49. Via oxide deposition (2000 Å + 5000 Å + 2000 Å)
50. Via hole definition (VI, Mask #12)
51. Via hole etching
52. Plug barrier2 TiN(1000 Å)
53. Plug deposition2 W(6000 Å)
54. Metal 2 sputtering [AlCu (18000 Å) / TiN (250 Å)]
55. Metal 2 definition (M2, Mask #13)
56. Metal 1 etching  

Fig. 3-8
57. Passivation oxide deposition (2000 Å)
58. Passivation Si$_3$N$_4$ deposition (7000 Å)
59. Pad definition (CB, Mask #14)
60. Alloy

Total photolithography steps: 14

§ 2 – 2 Typical CMOS layout example

(1) Well Masking -------
NW,PW

dark
outside: P-well (PW)

N-well (NW) clear
(2) Field-Oxide (Thin-Oxide) Masking

SN(OD)

SN(OD)

SN(OD)

(1A) P-Field Masking (PF)

SN(OD)

outside: P-well(PW)

SN(OD)

SN(OD)

PF dark

(3) Poly Masking

PO

SN(OD)

PO

PW

SN(OD)

SN(OD)

PO

NW
(4) N+ Masking
NM for NLDD and NP
N+ S/D

(5) P+ Masking
PM for PLDD and PP
P+ S/D

(6) Contact Masking
CO  shown in the above figure
§ 2-3 Layout Rules for Latchup

Parasitic p-n-p-n (SCR) structure in bulk CMOS:

\[ \text{Vin}_{\text{a}} \rightarrow \text{Vout} \rightarrow \text{VDD} \rightarrow \text{GND} \]
§ 2-3.1 Layout rule of MOS transistors for I/O parts or large driver (Based on 0.8μm layout rule)

1. NMOS transistor:
   
   (1) A P+ base guard ring should surround the NMOS. The P+ base guard ring must be connected to Vss by an unbroken metal line.
   
   (2) Maximum distance between surrounded P+ base guard ring is 80μm (e)
   
   (3) Minimum width of the P+ base guard ring is 4μm (a)
(4) Maximum distance between N+ source/drain areas and the nearest P+ well contact inside the P+ base guard ring must be less than 20μm (d). A butting contact is preferred if the process is allowed.

(5) N+ collector guard ring coupled with N-well should be placed outside the p-well region. The N+ guard ring must be connected to V_{SS} by an unbroken metal line.

(6) The minimum width of the N+ collector guard ring is 4μm(b).

(7) The minimum space between the P+ base guard ring and the N+ collector guard ring is 8μm(c).

(8) Minimum space between NMOS N+ collector guard ring and PMOS P+ collector guard ring is 30μm(f).

2. PMOS transistor:

(1) A N+ base guard ring should surround the PMOS. The N+ base guard ring must be connected to VDD by an unbroken metal line.

(2) Maximum distance between the surrounded N+ base guard ring is 80μm(e).

(3) Minimum width of the N+ base guard ring is 4μm (a)

(4) Maximum distance between P+ source/drain areas and the nearest N-well contact inside the N+ base guard ring must be less than 20μm(d). A butting contact is preferred if the process is allowed.

(5) P+ collector guard ring should be placed outside the N-well region. The P+ collector guard ring should be connected to V_{SS} by an unbroken metal line.
(6) Minimum width of the P⁺ collector guard ring is 4µm.
(7) Minimum space between N⁺ base guard ring and P⁺ collector guard ring is 8µm (c).

§ 2-3.2 Layout rule of internal circuits

(1) The internal circuit must be separated from I/O transistors with at least a double ring structure (with one N⁺ connected to VDD and one P⁺ connected to Vss).
(2) It is also recommended that large drivers are surrounded with a double guard ring structure.
(3) In an N-well (P-well), N-well (P-well) contacts should be used as many as possible. The maximum distance between a P⁺(N⁺) source/drain area and the nearest N-well (P-well) contact is 40µm.
Chapter 3  Current Sources and Simple Voltage Sources

§ 3-1  MOS Simple Current Sources

§ 3-1.1  NMOS Current Sources

1. MOS Widlar current mirror

(M₁) M₁:  \( V_{GS} = V_{DS} \Rightarrow V_{DS} > V_{GS} - V_{TH} \)  Both are sat.

M₂:  must be kept in the sat. region

i.e.  \( V_{out} > V_{GS} - V_{TH} \text{ or } V_{DSAT} \)

\[
I_{out} = I_{DS2} = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_2 (V_{GS2} - V_{TH2})^2 (1 + \lambda_2 V_{out})
\]

\[
I_{DS1} = I_{DS3} = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_3 (V_{GS1} - V_{TH1})^2 (1 + \lambda_1 V_{GS1})
\]

\[
I_{DS2} = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_2 (V_{GS2} - V_{TH2})^2 (1 + \lambda_2 V_{GS2})
\]

M₁ is identical to M₂ \( \Rightarrow V_{TH1} = V_{TH2} = V_{TH} \)

\( \lambda_1 = \lambda_2 = \lambda \)

\( \mu_n C_{ox} \text{ are the same} \)

\[
\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \frac{1 + \lambda V_{out}}{1 + \lambda V_{DS}}
\]

\( I_{DS1} = I_{DS3} = I_{REF} \text{ is called the reference current} \).

It can be generated by M₃ or other input circuits.
* If $\lambda \to 0 \Rightarrow \frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$

The output current $I_{out}$ depends only on the geometric ratio. $\Rightarrow I_{out}$ can be a constant current if $I_{REF}$ is a stable current.

$I_{out}$ is nearly independent of $V_{out}$ if $M_2$ is sat.

\[ * \quad r_o = \frac{r_{ds2}}{(\lambda I_{out})^{-1}} \quad L_2 \uparrow \Rightarrow r_o \uparrow \]

Remember:

```
\begin{align*}
\text{Ideal current source:} \\
\quad (1) \quad I = \text{constant, indep. of the loading and } V_{out} \\
\quad (2) \quad r_o = \infty.
\end{align*}
```

* To guarantee matched device characteristics, $L_1 = L_2$ is preferred and long channel devices are used. $W_1$ and $W_2$ should be kept large enough to avoid narrow channel effect.

* Can be used in the subthreshold poeration.

2. Cascode MOS Widlar current mirror

```
\begin{align*}
\text{Input Circuit} \\
\quad I_{REF} \\
\quad \text{Load} \\
\quad L_{out} \Rightarrow r_o \uparrow
\end{align*}
```
* $M_4$ and $M_2$ must be in the saturation region.

* $M_1/M_2$ ($M_3/M_4$) should have matched device characteristics.

* $M_4$ and $M_2$ must be in the sat. region

$\Rightarrow$ Large $V_{out}$ is required

$\Rightarrow$ The voltage swing of the load is limited especially for low $V_{DD}$.

* $r_o = r_{ds2} + r_{ds4} + r_{ds2} r_{ds4} (1 + \eta_d) g_{m4} \approx g_{m4} r_{ds2} r_{ds4}$

  High output resistance (by a factor of $g_{m4} r_{ds4}$)

  $\Rightarrow$ Long channel is used for $M_4$ to obtain a large $r_{ds4}$

* $I_{out} = \frac{(W/L)_2}{1 + \lambda V_{DS2}}$

  $I_{REF} = \frac{(W/L)_1}{1 + \lambda V_{GS}}$

  The output current is still determined by the bottom mirror.

* To guarantee $V_{GS} = V_{DS2}$ and matched device characteristics, $(W/L)_2/(W/L)_1 = (W/L)_4/(W/L)_3$ is used and $L_1=L_2=L_3=L_4$ is preferred. Thus $V_{GS3} = V_{GS4}$ and $V_{GS} = V_{DS2}$.

* Note that $M_3$ and $M_4$ have body effect

  $\Rightarrow V_{GS3}/V_{GS4} \uparrow$ and required $V_{out} \uparrow$

  $\Rightarrow (W/L)_3 > (W/L)_1$

  $\Rightarrow (W/L)_4 > (W/L)_2$ is adopted for compensation.

* The resistance seen from the input circuit is much smaller than $r_o \Rightarrow$ Inbalance $r_o$.

* Can be used in the subthreshold operation.

3.MOS Wilson current source
\[ I_{\text{out}} = \frac{(W / L)_2 \cdot I + \lambda V_{DS2}}{I_{\text{REF}} = \frac{(W / L)_3 \cdot I + \lambda V_{DS3}}{V_{DS2} = V_{GS}} \]
\[ V_{DS3} = V_{GS} + V_{GSI} \]
\[ V_{DS2} \neq V_{DS3} \]

* Inherent inbalance

\[ \Rightarrow \frac{I_{\text{out}}}{I_{\text{REF}}} \text{ depends on } V_{GS} \text{ and } V_{GSI} \]

\[ \Rightarrow \text{High precision ratio is not obtainable.} \]

\[ r_o \cong r_{ds1} + r_{ds1} \left[ \frac{g_{m1} g_{m3} (r_{ds3} \parallel r_{\text{OREF}}) + g_{m1}}{g_{m2} + \frac{I}{r_{ds2}} + g_{mb1}} \right] + \frac{I}{g_{m2} + \frac{I}{r_{ds2}} + g_{mb1}} \]

If \( r_{ds2} \gg \frac{I}{g_{m2}} \)

\[ \Rightarrow r_o = \frac{r_{ds1}}{g_{m2} + \frac{I}{r_{ds2}}} + r_{ds1} \left\{ \frac{g_{m1}}{g_{m2} + \frac{I}{r_{ds2}}} \right\} \left[ I + \left( \frac{g_{m1}}{g_{m2} + \frac{I}{r_{ds2}}} \right) \left( \frac{g_{m3} (r_{ds3} \parallel r_{\text{OREF}})}{g_{m2} + \frac{I}{r_{ds2}}} \right) \right] \]

\[ \equiv g_{m3} (r_{ds3} \parallel r_{\text{OREF}}) \left( \frac{g_{m1}}{g_{m2} + \frac{I}{r_{ds2}}} \right) r_{ds1} \]

Assume \( g_{m1} = g_{m2} = g_{m3} = g_m \) and \( \eta \to 0 \)
\[ r_o \approx \frac{I}{g_m} + r_{ds1} \left[ 2 + g_m \left( \frac{r_{ds3}}{r_{oref}} \right) \right] \]

\[ \approx r_{ds1} \left[ g_m \left( \frac{r_{ds3}}{r_{oref}} \right) \right] \]

* The output resistance is nearly the same as that of the cascoded current mirror.
* Only 3 MOS’s are used.
* Can be operated in the subthreshold region.

4. Improved Wilson current source

\[ \frac{I_{out}}{I_{REF}} = \frac{(W/L)_{2} + \lambda V_{GS2}}{(W/L)_{3} + \lambda V_{DS3}} \]

\[ V_{DS3} = V_{GS2} + V_{GS1} - V_{GS4} \]

Set \( V_{GS1} = V_{GS4} \) [i.e. \( \frac{(W/L)_{2}}{(W/L)_{4}} = \frac{(W/L)_{2}}{(W/L)_{3}} \)]

\[ \Rightarrow V_{DS3} = V_{GS2} \]

\[ \frac{I_{out}}{I_{REF}} = \frac{(W/L)_{2}}{(W/L)_{3}} \] precise ratio.

* Inherent balance like the cascode current source.

* High output resistance.

* 4 MOS’s are needed.

\[ \frac{(W/L)_{1}}{(W/L)_{4}} = \frac{(W/L)_{2}}{(W/L)_{3}} \Rightarrow V_{DS3} = V_{GS2} = V_{GS3} \]

and M3 sat.
* Better $r_o$ balance between load and $I_{\text{REF}}$ nodes.
* Can be used in the subthreshold operation.

5. High-swing cascode current source

A. Conventional type:

B. With source-follower level shifter:

$$I_{DS1} = I_{DS2} = \frac{W}{L} \frac{\mu_i C_{ox}}{2} (V_{TH} + \Delta V - V_{TH})^2$$

$$= \frac{I}{4} \frac{W}{L} \frac{\mu_i C_{ox}}{2} (V_{GS2} - V_{TH})^2$$

$$\Rightarrow V_{GS1} = V_{TH} + 2\Delta V$$
*High $r_0$.

*High output swing.

*Two extra MOS's.

$V_{DS1} = V_{TH} + \Delta V 
eq V_{DS2} = \Delta V$

Inbalance current ratio.

C. With constant $V_B$ bias circuit

$M_3$ in saturation:

$V_B - V_{TH3} \leq V_{GS1} (= V_x)$

$M_1$ in saturation:

$V_{GS1} - V_{TH1} \leq V_A (= V_B - V_{GS3})$

$⇒ V_{GS3} + (V_{GS1} - V_{TH1}) \leq V_B$

$≤ V_{GS1} + V_{TH3}$

$⇒ V_{GS3} - V_{TH3} \leq V_{TH1}$

or $\Delta V \leq V_{TH}$

If $V_B = V_{GS3} + (V_{GS1} - V_{TH1}) = V_{TH} + 2\Delta V$

$⇒ *$ The swing of load can be $V_{DD} - 2\Delta V$.

* $M_1$ and $M_2$ have the same $V_{DS}$ to obtain a precise current ratio.

The generation of $V_B$

$M_5 \equiv M_1 ⇒ V_{GS5} = V_{GS1}$

$⇒ (W/L)_6 < (W/L)_3$

$⇒ V_{GS6} > V_{GS3}$

$(W/L)_7$ is large

$V_{GS7} \equiv V_{TH7} > V_{TH1}$

Choose $(W/L)_6$ so that

$V_{GS6} - V_{GS7} = V_{GS3} - V_{TH1}$
§ 3-1.2 General Advantages of MOS Current Sources

1. Effective current gain $\beta \rightarrow \infty$

   $\Rightarrow$ No dc loading of slave stages on the master stage

   (Unlike the BJT multi-stage current mirrors)

2. Current ratio $\cong$ MOS channel geometric ratio

3. High packing density

4. $I_{out}$ can be as small as several nA.
   Generally, if $I_{out} < \sim nA$, leakage current dominates the output current

   $\Rightarrow$ The ratio is not constant anymore.

§ 3-1.3 PMOS/CMOS Current Sources

All NMOS current sources can be converted into PMOS current sources. They can be used in CMOS technology.

**Example: Multi-stage PMOS Widlar current source**
* $I_{out} > 10\mu A \Rightarrow V_{GS} > V_T$ and $I_D \propto (V_{GS} - V_T)^2$, square law

$\Rightarrow$ good ratio constancy.

§ 3-2 Supply – Independent Current Sources

§ 3-2.1 CMOS Peaking Current Source

CASE I: Subthreshold operation

In M1 and M3,

$I_{D01} = I_{D03}$, $V_{DS} >> V_t$

$V_{GS1} = I_{DS1} R + V_{GS3}$

$I_{DS1} = \left( \frac{W}{L} \right)_1 I_{D0} e^{V_{GS1} / V_t}$

$= \left( \frac{W}{L} \right)_1 I_{D0} e^{(I_{D0} R + V_{GS3}) / V_t}$

where $I_{D0} = I_{S0} / (W/L)$

$I_{out} = I_{D3} = \left( \frac{W}{L} \right)_3 I_{D0} e^{V_{GS3} / V_t}$
\[
\frac{I_{\text{out}}}{I_{\text{DS1}}} = \left(\frac{W}{L}\right)_{1} \exp \left(\frac{-R I_{\text{DS1}}}{n v_{t}}\right)
\]

\[
I_{\text{out}} = I_{\text{DS1}} \left(\frac{W}{L}\right)_{1} \exp \left(\frac{-R I_{\text{DS1}}}{n v_{t}}\right)
\]

\[
\frac{\partial I_{\text{out}}}{\partial I_{\text{DS1}}} = 0, \quad \frac{\partial^2 I_{\text{out}}}{\partial I_{\text{DS1}}^2} < 0 \Rightarrow I_{\text{DS1opt}} = \frac{n v_{\text{therm}}}{R}
\]

\[
\Rightarrow I_{\text{out max}} = \left(\frac{W}{L}\right)_{1} n v_{t} = \left(\frac{W}{L}\right)_{1} e R = \left(\frac{W}{L}\right)_{1} e
\]

* Power supply independent current with output current proportional to \(v_{t}\)
* Choose \(I_{\text{REF}} = I_{\text{DS1}} = I_{\text{DS1opt}}\), \(I_{\text{out max}}\) can be controlled by \(R\) or \((W/L)_{3}/(W/L)_{1}\)
* \(R\) can be implemented by the \(n^{+}\) source/drain diffusion.
  It can also be made by adjustable resistors.
* If \(I_{\text{REF}} = I_{\text{DS1opt}}\) has some inevitable variations, the resultant variations on
  \(I_{\text{out max}}\) is reduced because \(\partial I_{\text{out}}/\partial I_{\text{DS1}}\) arround \(I_{\text{DS1opt}}\) is very small.
* Two-stage peaking current sources can be used to further reduce the
  variations of \(I_{\text{out max}}\), \(I_{\text{out}}\) can be used to generate \(I_{\text{DS1opt}}\)
* Process variation and temperature coefficient (positive) on \(R\) should be considered.

CASE II: Saturation operation

\[
I_{\text{DS1}} = \frac{\mu_{n} C_{\text{ox}}}{2} \left(\frac{W}{L}\right)_{1} (V_{\text{GS1}} - V_{\text{TH}})^2
\]

\[
I_{\text{out}} = I_{\text{DS3}} = \frac{\mu_{n} C_{\text{ox}}}{2} \left(\frac{W}{L}\right)_{1} (V_{\text{GS3}} + I_{\text{DS1}} R - V_{\text{TH}})^2
\]

\[
I_{\text{out}} = \left(\frac{W}{L}\right)_{3} (V_{\text{GS3}} - V_{\text{TH}})^2 \frac{I_{\text{DS1}}}{(W/L)_{1} (V_{\text{GS3}} - V_{\text{TH}} + I_{\text{DS1}} R)^2}
\]

\[
\frac{\partial I_{\text{out}}}{\partial I_{\text{DS1}}} = 0, \quad \frac{\partial^2 I_{\text{out}}}{\partial I_{\text{DS1}}^2} < 0 \Rightarrow I_{\text{DS1opt}} = \frac{V_{\text{GS3}} - V_{\text{TH}}}{R}
\]

\[
\Rightarrow I_{\text{out max}} = \left(\frac{W}{L}\right)_{3} \frac{V_{\text{GS3}} - V_{\text{TH}}}{4R} = \left(\frac{W}{L}\right)_{1} \frac{1}{4} I_{\text{DS1opt}}
\]
* $I_{out \max}$ is power supply independent, but not proportional to $v_t$.

* Other features are the same as those in the subthreshold operations.

§ 3-2.2 CMOS $v_t$ Standard Current Source

M1, M2, M3 and M4 are operated in the subthreshold region.

CASE I:
M1 and M3 are in the same p-well

\[ V_{GS3} = V_{GS1} - V_R + \Delta V_{TH} \]
\[ V_{DS1} \gg v_t, V_{DS3} \gg v_t \]
\[ I_{DS1} = \left( \frac{W}{L} \right)_1 I_{DON} e^{\frac{V_{gs1}}{n_v}} \]
\[ = I_{DS2} = \left( \frac{W}{L} \right)_2 I_{DOP} e^{\frac{V_{gs2}}{n_v}} \]
\[ I_{DS4} = \left( \frac{W}{L} \right)_4 I_{DOP} e^{\frac{V_{gs4}}{n_v}} \]
\[ = I_{DS3} = \left( \frac{W}{L} \right)_3 I_{DON} e^{\frac{V_{gs3}}{n_v}} e^{-(v_a - \Delta V_{TH})/n_v} \]
\[ \Rightarrow e^{\frac{V_{gs2}}{n_v}} = \left( \frac{W}{L} \right)_2 e^{\frac{V_{gs1}}{n_v}} \\
\left( \frac{W}{L} \right)_4 \left( \frac{W}{L} \right)_2 e^{\frac{V_{gs4}}{n_v}} = \left( \frac{W}{L} \right)_3 e^{\frac{V_{gs3}}{n_v}} e^{-(v_a - \Delta V_{TH})/n_v} \]
\[ \Rightarrow V_R = n_v \ln \left[ \frac{W}{L}_3 \left( \frac{W}{L}_2 \right) \right] + \Delta V_{TH} \]

where \( \Delta V_{TH} = \text{GAMMA} \left( \sqrt{\phi_S + V_R - \sqrt{\phi_S}} \right) \)

CASE II:
M3 is in a separated well (special process) with $V_{BS}=0$, $V_{GS3} = V_{GS1} - V_R$
\[ V_R = nV_i \ln \left[ \frac{(W/L)_3}{(W/L)_2} \right] \]

\[ I_R = \frac{V_R}{R} \]

\[ I_{out} = [(W/L)_3/(W/L)_4] I_R \]

* The output current is power-supply independent.
* Since \( I_R \) is small enough, the start-up circuit is not necessary.
* \( R \) may be implemented by \( n^+ \) diffusion or adjustable resistors.
* Process variations on \( R \) should be considered.
* The temperature coefficient of \( R \) is usually positive. Thus \( I_R \) is not linearly proportional to temperature exactly.

§ 3-2.3 Constant – \( g_m \) Current Source

**All MOS devices are operated in the saturation region**

\[ V_{GS1} = V_{GS3} + I_D R \]

\[ I_{REF} = I_{DS1} = I_{out} \]

\[ I_{DS3} = K I_{DS1} \]

\[ I_{out} = \frac{2}{\mu_n C_{ox} (W/L)_1} \frac{1}{R^2} \left( 1 - \frac{1}{\sqrt{K}} \right)^2 \left( 2 \Delta V_{TH} + \frac{\Delta V_{TH}^2}{R} + \frac{\Delta V_{TH}^2}{I_{out} R^2} \right) \]

If \( \Delta V_{TH} \) is small

\[ g_{m\text{load}} = \sqrt{2 \mu_n C_{ox} (W/L)_1} I_{D1} \]

\[ = \sqrt{(W/L)_1} \frac{2}{R} \left( 1 - \frac{1}{\sqrt{K}} \right) \]
* The \( g_{\text{mload}} \) of the load NMOS device is independent of power supply voltages and depends upon \( R \) and channel geometric ratio.
* Both temperature coefficient and process variations of \( R \) still affect \( g_{\text{m}} \).
* \( R \) can be tuned to compensate its process variation.
* \( R \) can be realized by switched-capacitor resistors for better accuracy and tunability. However, clocks and capacitors are required.
* \( \Delta V_{\text{TH}} \) due to the body effect of \( M_3 \) causes error in \( I_{\text{out}} \).
* \( R \) can be moved to the source of \( M_4 \) to avoid the body effect.

\[ \therefore \text{PMOS in 0.5\textmu m CMOS process can have separate n-wells.} \]

** Requires start-up circuit to stabilize the circuit as \( V_{\text{DD}}/V_{\text{SS}} \) is powered up. Adding \( C_{\text{start}} \) is a simple way to perform start-up.
* Requires careful HSPICE simulation and analysis for the start-up circuit.

Transient analysis using the ramp \( V_{\text{DD}} \) waveform.

\[ V_{\text{DD}} \]

0

§3-3 Simple MOS Voltage Sources (For capacitive loads only)

\[ V_{\text{GS}} = V_{\text{DS}} \]
\[ V_{\text{DS}} = V_{\text{GS}} > V_{\text{GS}} - V_{\text{T}} \]
always saturation in long-channel or short-channel devices

(2) PMOS version

* For 0.5\textmu m CMOS technology all substrates are the same p-type semiconductor connected to ground or \(-V_{\text{SS}}\).
\[ \Rightarrow \text{Body effect in } M_{N1} \text{ and } M_{N2} \]

* For PMOS version, separate n-wells can be used.
\[ \Rightarrow \text{No body effect, but larger chip area.} \]

* \( V_{\text{DD}} + V_{\text{SS}} > V_{\text{THM1}} + V_{\text{THM3}} + V_{\text{THM2}} \)

* \( I_{\text{VD}} = I_{\text{VSS}} \propto V_{\text{DD}} + V_{\text{SS}} \)

* \( M_{N1}, M_{N2}, \text{ and } M_{N3} \) may have different channel dimensions.

* Output resistance \( \propto 1/g_{\text{m}} \)
(3) NMOS-PMOS combinations

e.g. +VDD.

\[\begin{align*}
\text{MP}_1 & \quad \text{V}_3 \\
\text{MN}_1 & \quad -V_{SS}
\end{align*}\]

\[\begin{align*}
\text{MP}_1 & \quad \text{V}_4 \\
\text{MP}_2 & \quad \text{V}_5 \\
\text{MN}_1 & \quad -V_{SS}
\end{align*}\]

**Ideal Voltage Source:**

(1) \( Rs = 0 \)

(2) \( V_{out} = V = \text{constant} \) independent of current loading.
Chapter 4   CMOS Amplifiers, Level Shifting Circuits, and Output stages

4-1 Active-Load MOS Amplifiers

4-1.1 NMOS Amplifiers

1. Simple NMOS common-source amplifier

\[ v_o > v_i - V_{TH1} \text{(or } V_{DSAT1} \text{)} \]

* \( M_1 \) and \( M_2 \) must be always biased in the saturation region.

* \( M_1 \) sat \( \Rightarrow v_o \geq V_{DSAT1} \leq v_i - V_{TH1} \)

* \( M_2 \) sat \( \Rightarrow V_{DD} - v_o \geq V_{DSAT2} \leq V_{GG} - V_{TH2} - v_o \)

* \( V_{GG} < V_{DD} + V_{TH2} \Rightarrow V_{GG} < V_{DD} \)

Transfer characteristic:

Assume \( \lambda \to 0 \), \( \text{GAMMA} \to 0 \), and the same \( \mu_n C_{ox} \)

\[ \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_1 (v_i + V_{SS} - V_{TH2})^m = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_2 \left( V_{GG} - v_o - V_{TH2} \right)^m, I \leq m \leq 2 \]

\( \Rightarrow v_o = V_{GG} - \left( \frac{W/L_1}{W/L_2} \right)^l (v_i + V_{SS} - V_{TH2}) - V_{TH2} \)

\[ V_{ODC} \propto V_{IDC} \]
At point A, \( v_{IA} = v_{OA} + V_{TH1} \)

\[
v_{OA} = \left( V_{GG} - V_{TH2} - \left( \frac{W/L}{L} \right)^{\frac{l}{2}} V_{SS} \right) I + \left( \frac{W/L}{L} \right)^{\frac{l}{2}}
\]

The range of \( v_o \) in which both MOS are in the saturation region is

\[
V_{GG} - V_{TH2} > v_o \geq \left( V_{GG} - V_{TH2} - \left( \frac{W/L}{L} \right)^{\frac{l}{2}} V_{SS} \right) I + \left( \frac{W/L}{L} \right)^{\frac{l}{2}}
\]

\[
A_v = \frac{\partial v_o}{\partial v_i} = -\left( \frac{W/L}{L} \right)^{\frac{l}{2}} \quad , \quad (W/L)_i < 1 \quad \text{for high } A_v
\]

The range for \( v_i \) is

\[
-V_{SS} + V_{TH1} \leq v_i \leq V_{GG} - V_{TH2} - \left( \frac{W/L}{L} \right)^{\frac{l}{2}} V_{SS} + V_{TH1} \quad \text{(or } v_{IA})
\]

Small-signal model:

\[
A_v = \frac{v_o}{v_i} = -\frac{g_{m1}}{g_{m2} + g_{mb2} + \frac{l}{r_{ds1} \| r_{ds2}} \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}}
\]

\[\text{if } (g_{m2} + g_{mb2}) \gg \frac{l}{r_{ds1} \| r_{ds2}}\]

\[
A_v = -\frac{g_{m1}}{g_{m2}} \cdot \frac{l}{l + \eta_2} = -\alpha \frac{g_{m1}}{g_{m2}}
\]
where \( \eta_2 = \frac{\text{GAMMA}_2}{2\sqrt{V_{bb} + v_o + \phi_s}} \) and \( \alpha_2 = \frac{l}{l + \eta_2} \).

\( g_m = 2 \sqrt{\frac{\mu c_m}{2}} \left( \frac{W}{L} \right) I_{DS} \) or \( m \left( \frac{\mu c_m}{2} \frac{W}{L} I_{DS} \frac{L}{m-l} \right)^{\frac{1}{m}} \)

\( \Rightarrow A_v = -\alpha_2 \sqrt{\frac{(W/L)}{(W/L)_2}} \) or \( -\alpha_2 \left( \frac{(W/L)}{(W/L)_2} \right)^{\frac{1}{m}} \), \( 1 < m < 2 \)

If \( \eta_2 \ll 0 \) , \( \alpha_2 = 1 \) . \( (\text{GAMMA}_2 \downarrow , V_{bb} + v_o \uparrow \Rightarrow \eta_2 \downarrow) \)

\( \Rightarrow A_i = -\sqrt{\frac{(W/L)}{(W/L)_2}} \) or \( \left[ \frac{(W/L)}{(W/L)_2} \right]^{\frac{1}{m}} \)

* The voltage gain is determined by the geometric ratio.

Example: \( (W/L)_1 = 10 \) \( (W/L)_2 = 0.1 \) \( \alpha_2 = 1 \)

\( \Rightarrow A_i = -\sqrt{100} = -10 \)

* The body effect of M_2 degrades the voltage gain.

* The dc output voltage is dependent on the input dc bias voltage or equivalently the dc operating current.

2. NMOS inverter without \( V_{GG} \)

Amplifier range:

\[ V_{DD} - V_{TH2} > v_o \geq \left( V_{DD} - V_{TH1} - \left( \frac{(W/L)}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right) \]

\[ \text{or } V_{DSAT1} \]

\[ \frac{I}{I + \left( \frac{(W/L)}{(W/L)_2} \right)^{\frac{1}{m}}} \]
\[-V_{SS} + V_{TH1} \leq i_v \leq \frac{V_{DD} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{i_v}{V_{SS}}}V_{SS}}{I + \left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{i_v}{V_{SS}}}} + V_{TH1} \quad \text{or} \quad v_{IA}\]

\[V_{ODC} = V_{DD} - \left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{i_v}{V_{SS}}} \left(V_{DC} + V_{SS} - V_{TH1}\right) - V_{TH2}\]

* No extra power supply \(V_{GG}\) is required.

* \(A_v = -\alpha \left(\frac{(W/L)_1}{(W/L)_2}\right) \Rightarrow (W/L)_2 < 1 \quad \text{for high} \ A_v\]

3. Split-Load inverter

Single \(M_2 \Rightarrow (W/L)_2 << 1 \quad \text{very long channel device}\)

\[C_{gs2} = \frac{2}{3} C_{os}(L \cdot W)_2 = \frac{2}{3} \frac{W^2}{(W/L)_2}\]

\[(W/L)_2 << 1 \Rightarrow C_{gs2} \uparrow\]

\[f_{-3\text{db}} = \frac{1}{2\pi \frac{1}{g_{m2}} C_{gs2}} = \frac{3I_{DS}^2}{2\pi \mu \frac{C_{os}}{2} W^2 C_{os}(V_{GS2} - V_{TH2})}\]

\[I_{DS} \uparrow \Rightarrow f_{-3\text{db}} \uparrow \quad ; \quad C_{gs2} \uparrow \Rightarrow f_{-3\text{db}} \downarrow\]
4. NMOS Cascode amplifier

If $I_{DS1} = I_{DS2}$

$$A_{ij} = \frac{V_{DL}}{V_i} = -\alpha \frac{g_{m1}}{g_{m2}} = -\alpha \left[\frac{(W/L)_i}{(W/L)_2}\right]^{\nu/n}$$

If $I_{DS1} = I_{DS3}$

$$A_i = \frac{V_{OL}}{V_i} = -\alpha \frac{g_{m1}}{g_{m3}} = -\alpha \left[\frac{(W/L)_i}{(W/L)_3}\right]^{\nu/n}$$

$$C_{in} = C_{gr1} + C_{gd1} \left(1 + \frac{g_{m1}}{g_{m2}}\right)$$

If $g_{m1} = g_{m2}$

$$\Rightarrow C_{in} = C_{gr1} + 2C_{gd1}$$

$$C_{in} \propto g_{m1}/g_{m2}$$

* Design considerations:

1. $\left[\frac{W}{L}\right]_1 = \left[\frac{W}{L}\right]_2 \Rightarrow g_{m1} = g_{m2}$ (Neglecting the body effect of M2)
   Keep $C_{in}$ Small, Miller Effect $\downarrow$

2. $\left[\frac{W}{L}\right]_3 \ll \left[\frac{W}{L}\right]_i \Rightarrow g_{m3} \ll g_{m1}$, Voltage gain $A_v \uparrow$
(3) $V_{DS2}(V_{DS1})$ must be large enough to keep $M_2(M_1)$ sat.

* $g_{m1} < g_{m2} \Rightarrow A_{seq} < 1 \Rightarrow$ Smaller Miller effect

But $\left(\frac{W}{L}\right)_1 < \left(\frac{W}{L}\right)_2$ is not recommended.

\[ V_{DS1} \text{ will become smaller } \Rightarrow M_1 \text{ may not be in the sat. region.} \]

* $\left(\frac{W}{L}\right)_2 > \left(\frac{W}{L}\right)_1$ slightly to compensate the body effect of $M_2$.

5. MOS source-couple pair

\[
I_{DS1} = \left(\frac{\mu_n C_{ox}}{2}\right)_1 \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2
\]

\[
I_{DS2} = \left(\frac{\mu_n C_{ox}}{2}\right)_2 \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2
\]

\[
I_{DS1} + I_{DS2} = I_{SS}
\]

\[
V_{GS1} = V_{I1} - V_S
\]

\[
V_{GS2} = V_{I2} - V_S
\]

Assume identical devices

i.e. $V_{TH1} = V_{TH2}, \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ and $\left(\frac{\mu_n C_{ox}}{2}\right)_1 = \left(\frac{\mu_n C_{ox}}{2}\right)_2 = \frac{\mu_n C_{ox}}{2}$

\[ \Rightarrow \Delta I_{DS} \equiv I_{Dn1} - I_{Dn2} = \frac{\mu_n C_{ox} W}{2} \left(\frac{2I_{SS}}{L} - (\Delta V_i) \right) \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W}} \]

where $\Delta V_i \equiv V_{I1} - V_{I2}$ (input differential voltage)

If $\Delta V_i \leq \sqrt{\frac{I_{SS}}{\mu_n C_{ox} W}} \frac{L}{2}$

\[ \Rightarrow \Delta I_D \propto \Delta V_i, \text{linear range} \]

\[ \Rightarrow \text{between } + \frac{I_{SS}}{2} \text{ and } - \frac{I_{SS}}{2}. \]

Linear range $\propto \sqrt{I_{SS} \frac{L}{W}}$

Typically, $\Delta V_i \approx \pm 300 \text{mV}$ to

$\pm V$ in the linear range,

Larger than that of the emitter-couple pair.
\[ G_m \equiv \frac{\partial \Delta I_{DS}}{\partial \Delta V_t}_{\Delta V_t=0} = \left( \frac{\mu_n C_{ox}}{2} \frac{W}{L} \right) \sqrt{\frac{2I_{ss}}{\mu_n C_{ox} \frac{W}{L}} - (\Delta V_t)^2} - \frac{\mu_n C_{ox}}{2} \frac{W}{L} \Delta V_t \]

\[ \Delta V_t = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox} \frac{W}{L}} - (\Delta V_t)^2} \]

\[ = 2 \sqrt{\frac{I_{ss} \mu_n C_{ox} \frac{W}{L}}{2}} = g_{m1} \text{ or } g_{m2} \]

\[ = \sqrt{I_{ss} \mu_n C_{ox} \frac{W}{L}} \]

* Gm is the differential output transconductance
  Gm at \( \Delta V_t=0 \) is the maximum.

* If operated in the subthreshold region, Gm max = \( g_{m1} \) or \( g_{m2} = \frac{I_{DS}}{nv_t} \)

6. NMOS differential stage

![NMOS differential stage diagram]

DC considerations:

(1) Transfer characteristic:

(\( W/L \))\(_1\) = (\( W/L \))\(_2\)  \( (W/L)_3 = (W/L)_4 \)

Source-coupled pair \( M_1 \) and \( M_2 \)
\[ \Rightarrow \Delta I_{DS} \equiv I_{DS1} - I_{DS2} = \left( \frac{\mu_n C_{ox} W}{2 L} \right) \left( \Delta V_1 \right) \sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{ox} W}{2 L}}} - (\Delta V_1)^2 \]

where \( \Delta V_1 \equiv V_{i1} - V_{i2} \)

\[ I_{DS1} = I_{DS1} = \frac{\mu_n C_{ox} (W/L)}{2} (V_{DD} - V_{o1} - V_{TH3})^2 \]

\[ I_{DS4} = I_{DS4} = \frac{\mu_n C_{ox} (W/L)}{2} (V_{DD} - V_{o2} - V_{TH4})^2 \]

\[ V_{o1} = V_{DD} - V_{TH3} - \sqrt{\frac{I_{DS1}}{2 \mu_n C_{ox} (W/L)}} \quad V_{o2} = V_{DD} - V_{TH4} - \sqrt{\frac{I_{DS2}}{2 \mu_n C_{ox} (W/L)}} \]

\[ \Delta V_o \equiv V_{o1} - V_{o2} = V_{TH4} + \frac{I_{DS1}}{2 \mu_n C_{ox} (W/L)} - V_{TH3} - \frac{I_{DS2}}{2 \mu_n C_{ox} (W/L)} \]

\[ = (V_{TH4} - V_{TH3}) + \frac{1}{\sqrt{\frac{I_{SS}}{2 \mu_n C_{ox} (W/L)^2}}} \left( \sqrt{\frac{I_{SS}}{2} + \frac{\Delta I_{DS}}{2}} - \sqrt{\frac{I_{SS}}{2} + \frac{\Delta I_{DS}}{2}} \right) \]

\[ = f(I_{SS}, \Delta V_1) \]

\[ \Rightarrow \Delta V_o \text{ vs } \Delta V_1 \text{ is the voltage transfer characteristic.} \]

(2) Input voltage limits:

Positive maximum common-mode voltage \( V_{ICM}^+ \)

\[ V_{ICM}^+ = V_{o1} + V_{TH1} = V_{DD} - V_{TH3} - \sqrt{\frac{I_{SS}}{2 \mu_n C_{ox} (W/L)^2}} + V_{TH1} \]

(long-channel device)

\( V_{ICM}^+ \text{ such that } V_{O1} - V_s = V_{DSAT1} \) (short-channel device)

(M1 and M2 sat.)

Negative maximum common-mode voltage \( V_{ICM}^- \)

M5 must be sat.
\[ V_{ICM}^- = V_{BS} + V_{TH5} + \sqrt{\frac{I_{SS}}{2}} \left( \frac{\mu C}{2} \right) \left( \frac{W}{L} \right)_1 + V_{TH1} \]

(long-channel device)

\[ V_{ICM}^- \text{ such that } V_S + V_{SS} = V_{DSAT5} \quad \text{(short-channel device)} \]

Positive maximum differential voltage \( V_{ID}^+ \)

\[ V_{ID}^+ = V_{DD} - V_{TH3} + \sqrt{\frac{I_{SS}}{2}} \left( \frac{\mu C}{2} \right) \left( \frac{W}{L} \right)_3 + V_{TH1} \]

(long-channel device)

\[ V_{ID}^+ \text{ such that } V_{O1} - V_S = V_{DSAT1} \quad \text{(short-channel device)} \]

(Keep M1 or M2 sat.)

Negative maximum differential voltage \( V_{ID}^- \)

\[ V_{ID}^- = -V_{ID}^+ \]

(3) Input offset voltage

\[ V_{OS} \equiv V_{GS1} - V_{GS2} \bigg|_{V_{BS}} \]

\[ = \sqrt{\frac{I_{DS1}}{\left( \frac{\mu C}{2} \right)_1 \left( \frac{W}{L} \right)_1}} + V_{TH1} - \sqrt{\frac{I_{DS2}}{\left( \frac{\mu C}{2} \right)_2 \left( \frac{W}{L} \right)_2}} - V_{TH2} \]

\[ V_{O1} = V_{O2} = V_O = V_{DD} - V_{TH3} - \sqrt{\frac{I_{DS1}}{\left( \frac{\mu C}{2} \right)_3 \left( \frac{W}{L} \right)_3}} \]

\[ = V_{DD} - V_{TH4} - \sqrt{\frac{I_{DS1}}{\left( \frac{\mu C}{2} \right)_4 \left( \frac{W}{L} \right)_4}} \]

\[ \Rightarrow \sqrt{I_{DS1}} = \sqrt{\left( \frac{\mu C}{2} \right)_3 \left( \frac{W}{L} \right)_3 (V_{DD} - V_{TH3} - V_O)} \]

\[ \sqrt{I_{DS2}} = \sqrt{\left( \frac{\mu C}{2} \right)_4 \left( \frac{W}{L} \right)_4 (V_{DD} - V_{TH4} - V_O)} \]
\[ V_{ds} = \left[ \frac{\mu_{c, ox}}{2} \left( \frac{W}{L} \right) \right] (V_{dd} - V_{o} - V_{th1}) \]

\[ - \left[ \frac{\mu_{c, ox}}{2} \left( \frac{W}{L} \right) \right] (V_{dd} - V_{o} - V_{th4} + (V_{th1} - V_{th2}) \]

Define \( \Delta X_2 = X - X_2 \quad X_2 = -X + X_2 \)

\[ \Rightarrow X_1 = X_{12} + \frac{\Delta X_{12}}{2} \quad X_2 = X_{12} - \frac{\Delta X_{12}}{2} \]

\[ V_{os} = \left[ \frac{\mu_{c, ox}}{2} \left( \frac{W}{L} \right) \right] (V_{dd} - V_{o} - V_{th34}) \left[ \frac{\Delta \left( \frac{\mu_{c, ox}}{2} \right)}{2} \left( \frac{W}{L} \right) \right] + \frac{\Delta \left( \frac{W}{L} \right)}{2} \]

\[ - \frac{\Delta \left( \frac{\mu_{c, ox}}{2} \right)}{2} \left( \frac{W}{L} \right) - \frac{\Delta V_{th34}}{V_{dd} - V_{o} - V_{th34}} + \Delta V_{th12} \]

\[ = \frac{I_{ds}}{\frac{\mu_{c, ox}}{2} \left( \frac{W}{L} \right)} \left[ \frac{\Delta W_{34}}{2W_{34}} + \Delta L_{12} \right] + \left[ \frac{\Delta W_{34}}{2W_{34}} - \Delta W_{12} \right] - \frac{\Delta V_{th34}}{V_{gs12} - V_{th12}} \left[ \frac{\Delta W_{34}}{2W_{34}} + \Delta L_{12} \right] - \frac{\Delta V_{th34}}{V_{gs12} - V_{th12}} \]

\[ \Rightarrow \Delta V_{th12} + (V_{gs12} - V_{th12}) \left[ \frac{\Delta W_{34}}{2W_{34}} + \Delta L_{12} \right] - \frac{\Delta V_{th34}}{V_{gs12} - V_{th12}} \]
* If $\Delta V_{th}$ is large and the differential gain is high,

$$V_{os} \approx \Delta V_{th12}$$

* If $\frac{\Delta W}{2W}$ and $\frac{\Delta L}{2L}$ is large, keep $V_{gs12} - V_{th12}$ small.

$$\Rightarrow V_{os} \approx (V_{gs} - V_{th12})(\frac{\Delta W_{3d}}{2W_{3d}} + \frac{\Delta L_{12}}{2L_{12}})$$

$V_{os} \propto$ input overdrive voltage

* If operated in the subthreshold region,

$$I_{ds} \propto \exp\left(\frac{V_{gs}}{nV_t}\right)$$

$V_{os}$ is smaller than that operated in the saturation region.

This case is similar to the BJT case. \: $\therefore V_{os} \propto \Delta I_{ds}$

(3) AC Gain

**Differential signal**

**Common-mode signal**

Half-Circuit concept:

$$A_{dm} \equiv \frac{V_{vd}}{V_{id}} = -\alpha_{m} \frac{g_{m1}}{g_{m3}}$$
Common-mode half-circuit:

\[ V_{bias} \xrightarrow{M_5} \frac{I}{2} M_5 \xrightarrow{\frac{1}{2} g_{ds}} \]

\[ A_{cm} \equiv \frac{V_{in}}{V_{ic}} = -\alpha_1 \alpha_2 \frac{g_{ds}}{2 g_{m1}} \]

\[ CMRR \equiv \frac{A_{in}}{A_{cm}} = \frac{2 g_{m1}}{g_d \alpha_1} \]

* \( L_5 \uparrow \Rightarrow g_{ds} \downarrow \Rightarrow CMRR \uparrow \)

* When cascoded current source is used for Iss, \( g_{ds} \downarrow \Rightarrow CMRR \uparrow \)

But \( V_S \uparrow \Rightarrow \) common-mode range \( \downarrow \)

7. NMOS source follower
   The voltage gain (midband) is
   \[ A_i = \frac{g_{m1}}{g_{m1} + \frac{1}{\alpha_1 r_{ds1}} + \frac{1}{r_{ds2}}} < 1 \]
   If \( r_{ds1}, r_{ds1} \gg \frac{\alpha_1}{g_{m1}} \)
   \[ \Rightarrow A_i = \alpha_i < 1, \] smaller than that of the emitter follower.

8. NMOS differential-input to single-ended converter
\[ A_v = \frac{N + 1}{2} = \frac{\alpha_3}{1 + \frac{\alpha_3}{g_{m3}} \left( \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} \right)} \left( = \frac{v_o}{v_{il} - v_{i2}} \right) \]

where \[ N = \frac{g_{m1} g_{m2}}{g_{m3} \left( \frac{g_{m1}}{\alpha_1} + g_{m2} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} \right)} \]

If \( M_2 \equiv M_4, M_3 \equiv M_1, \frac{1}{r_{ds}} \ll g_m \)

\[ \Rightarrow g_{m2} = g_{m4}, g_{m3} = g_{m1} \]

\[ N \equiv \frac{g_{m4}}{g_{m4} + \frac{g_{m3}}{\alpha_3}} \]

\[ A_v \equiv \frac{\alpha_3}{2g_{m4} + \frac{g_{m3}}{\alpha_3}} < 1 \]

\[ CMRR = \frac{1 + N}{2(1 - N)} = \frac{1 + \frac{g_{m4}}{g_{m3}/\alpha_3}}{2} \]

To obtain a large CMRR, \( g_{m4} \gg \frac{g_{m3}}{\alpha_3} \)

\[ \Rightarrow A_v \equiv \frac{\alpha_3}{\alpha_3} < 1 \]

§ 4-1.2 CMOS Amplifier

1. Simple common-source amplifier

M_2 : PMOS current source

\[ M_1 \text{ and } M_2 \text{ sat. } \Rightarrow V_{BIAS} + |V_{TH1}| > v_o > v_i - V_{TH1} \text{ or } V_{DD} - |V_{DSAT2}| \geq V_o \geq V_{DSAT1} - V_{SS} \]
\[ A_v = -g_{m1} \left( r_{ds1} / r_{ds2} \right) \]

\[ g_{m1} = \sqrt{2I_{DS1}\mu_n C_{ox} \frac{W}{L}} \], \( r_{ds1} = \frac{1}{\lambda I_{S1}} \), \( r_2 = \frac{1}{\lambda I_{S2}} \)

\[ A = \frac{1}{\sqrt{I_{DS1}}} \left( \frac{1}{\lambda_1 + \lambda_2} \right) \sqrt{2\mu C \frac{W}{L}} \]

\[ |A_v| \approx \frac{1}{\sqrt{I_{DS1}}} \quad \text{(long-channel devices)} \]

\[ |A_v| \approx \left( I_{DS1} \right)^{\frac{1}{m}} \quad \text{(short-channel devices)} \]

Output resistance \( r_o \), \( r_o = r_{ds1} / r_{ds2} \)

---

2. Complementary CMOS common-source amplifier

Assume \( V_{TH1} = V_{TH2} = V_{TH} \)

If \( v_i - V_{TH} < v_o < v_i + V_{TH} \) or \( V_{DD} - |V_{DSAT2}| \geq v_o \geq V_{DSAT1} - V_{SS} \)

\[ A_v = -\left( g_{m1} + g_{m2} \right) \left( r_{ds1} / r_{ds2} \right) \]

\[ r_o = r_{ds1} / r_{ds2} \]

*Higher gain than the circuit in 1.

*Narrow operating range.

---

3. Complementary inverter with level shifter.

\( M_2 \) sat. \( \Rightarrow V_{DD} - v_i - V_{TH} < V_{DD} - v_o \)

\( M_1 \) sat. \( \Rightarrow v_i - V_{SH} + V_{SS} - V_{TH} < v_o + V_{SS} \)

\[ \Rightarrow v_i - V_{TH} - V_{SH} < v_o < v_i + V_{TH} \]

* \( r_o = r_{ds1} / r_{ds2} \)

* The range of \( v_o \) is increased by \( V_{SH} \).

* In the short-channel case, \( V_{GS1} \downarrow \text{ by } V_{SH} \), \( V_{DSAT1} \downarrow \Rightarrow \) The range is also increased.
4. Cascode amplifier with PMOS current-source load

\[ A_v = -g_{m1} \left[ r_{ds3} \parallel \left( \frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2} \right) \right] \]

\[ \equiv -g_{m1} r_{ds3} \]

\[ r_o = r_{ds3} \parallel \left( \frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2} \right) \]

\[ \equiv r_{ds3} \]

* PMOS devices can be used as cascode amplifier whereas NMOS device as current source.

5. Cascode amplifier with PMOS cascode current-source load

\[ A_v = -g_{m1} \left[ \left( \frac{1}{\alpha_3} g_{m3} r_{ds4} r_{ds3} \right) \parallel \left( \frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2} \right) \right] \]

\[ \equiv -\frac{1}{2\alpha} g_{m1} g_{m3} r_{ds}^2 \]

if \( \alpha_3 = \alpha_2 = \alpha \)

\( g_{m3} = g_{m2} = g_m \)

\( r_{ds4} = r_{ds3} = r_{ds2} = r_{ds1} = r_{ds} \)

\[ r_o \equiv \frac{1}{2\alpha} g_m r_{ds}^2 \]

* Larger \( r_o \) and \( A_v \)

* Limited output voltage swing

\( \Rightarrow \) High-swing cascode current source is preferred

6. Folded cascode amplifier

M1: CS amplifier

M2: CG amplifier

Optimal operating point:

\[ I_{DS1} = I_{DS2} = \frac{1}{2} = I_{DS3} \]

\( g_{m1} = g_{m2} \)

(to avoid large Miller capacitance at input)

\[ A_v = -g_{m1} \left\{ r_{ds3} \parallel \left( g_{m2} (r_{ds1} \parallel r_{ds1}) r_{ds2} \right) \right\} \]

\[ \equiv -g_{m1} r_{ds3} \]
7. Improved cascode amplifier with current injection circuitry

conventional cascode amplifier

\[ A_v \equiv -g_{m1} r_{ds3} \propto \frac{1}{\sqrt{I_{DS}}} \]

\[ I_{DS} \downarrow \Rightarrow A_v \uparrow \text{ until subthreshold} \]

M3: current source as load
M4: current-injection current source

\[ A_v \equiv -g_{m1} r_{ds3} \propto \frac{\sqrt{I_{DS4}}}{\sqrt{I_{DS}}} \]

To increase \( A_v \) \( \Rightarrow \) \( I_{DS4} \uparrow \) and \( I_{DS} \downarrow \)

* Higher voltage gain and the same \( r_o \)
* Extra device M4 and extra power dissipation
* Firstly, design the circuit of M1, M2, and M3. Then add M4. Readjust the
  channel dimensions to keep the dc bias so that all devices are in saturation.

8. Differential amplifier with PMOS load

Half-circuit method can be used

\[ v_{id} \equiv v_{i1} - v_{i2} , \quad v_{ic} \equiv \frac{v_{i1} + v_{i2}}{2} \]

\[ v_{od} \equiv v_{o1} - v_{o2} , \quad v_{oc} \equiv \frac{v_{o1} + v_{o2}}{2} \]

\[ A_{dm} \equiv \frac{v_{od}}{v_{id}} \equiv -g_{m1} \frac{1}{g_{m3}} \]

\[ A_{cm} \equiv \frac{v_{oc}}{v_{ic}} \equiv -\alpha_n \frac{g_{ds}}{2g_{m3}} \]
CMRR \equiv \frac{A_{dm}}{A_{cm}} \equiv \frac{2g_{m1}}{g_{d5} \cdot \alpha_i}

r_{od} \equiv \frac{1}{g_{m3}}

r_{oc} \equiv \frac{1}{g_{m3}}

*Matched devices for \( \frac{M_1}{M_2} \) and \( \frac{M_3}{M_4} \)

*A_{cm} < 1 \) can be achieved

9. Different amplifier with PMOS current-source load

\( M_3, M_4 \): Two slave stages of the current mirror

\( \Rightarrow \) current-source load

\[ A_{dm} \equiv -g_{m1} (r_{ds1} \parallel r_{ds3}) \]

\[ A_{cm} \equiv -\frac{\alpha_i}{2r_{ds5}} (r_{ds3} \parallel g_{m1}r_{ds5}r_{ds1}) \]

CMRR \equiv \frac{2g_{m1} (r_{ds1} \parallel r_{ds3})r_{ds5}}{\alpha_i r_{ds3}}

* \( g_{m1} \uparrow , r_{ds5} \uparrow \Rightarrow \) CMRR \uparrow

* \( A_{cm} < 1 \) is preferred \( \Rightarrow r_{ds5} > r_{ds3} \)

* \( I_{SS} \) can be realized by cascode or high-swing cascode current source to increase

\[ r_{ds5} \left( = \frac{1}{g_{d5}} \right) \]

10. Differential amplifier with PMOS current injection circuit

If \( I_{SS} \) remains unchanged, \( g_{m1}=g_{m2} \) the same.

But \( g_{m3}=g_{m4} \) is reduced by \( \frac{1}{\sqrt{2}} \) if

\( I_{DS3} = I_{DS4} \) is reduced by half.

\( \Rightarrow A_{dm} \uparrow \text{ by } \sqrt{2} \)
\[ r_{ds7} = r_{ds8} \gg \frac{1}{gm3} = \frac{1}{gm4} \]

CMRR is the same.

* If \( M_1 \) and \( M_4 \) are current-source loads, could \( A_{dm} \) be increased? Why?

11. Differential cascode amplifier

\[ V_o \equiv V_{o1} - V_{o2} \]
\[ V_1 \equiv V_{i1} - V_{i2} \]

*Higher \( A_{dm} \)

*4 MOS devices stacked \( \left( M_1, M_3, I_{ss}, \frac{1}{2} I_{ss} \right) \)

\[ V_{DD} + V_{ss} \] might not be enough to maintain all the devices in saturation when low supply voltage is used.

12. Differential Folded cascode amplifier

*To retain the characteristics of cascode amplifier, the optimal design is
\[ I_{DD} = I_{ss} \]
\[ I_L = \frac{1}{2} I_{ss} \]

* Only 3 MOS devices stacked

\[ \Rightarrow \] low voltage operation is possible

* \( V_{ICM} \) ↑ why?
13. CMOS differential-input to single-ended-output converter.

Version 1: NMOS input

DC operating point:
It is better to keep $V_{\text{ODC}} \approx V_{\text{DD}} - V_{\text{GSI}}$
for better current-mirror balance.

Common-mode range:

$$V_{\text{ICM}}^+ = V_{\text{DD}} + V_{\text{THN}} - V_{\text{GSI}}$$

$$= V_{\text{DD}} + V_{\text{THN}} - \frac{I_o}{2} \left[ \mu_p C_{\text{oxn}} \left( \frac{W}{L} \right) \right] - |V_{\text{THP}}|$$

$$V_{\text{ICM}}^- = V_{\text{GSI}} + V_{\text{BIAS}} - V_{\text{THN}}$$

$$= \frac{I_o}{2} \left[ \frac{\mu_p C_{\text{oxn}}}{2} \left( \frac{W}{L} \right) \right] + V_{\text{BIAS}}$$

Differential-mode range:

$$V_{id}^+ = -V_{id}^- = V_{\text{DD}} + V_{\text{THN}} - \frac{I_o}{2} \left[ \mu_p C_{\text{oxn}} \left( \frac{W}{L} \right) \right] - |V_{\text{THP}}|$$

$$v_{in1} = \frac{v_{id}}{2} + v_{ic}$$

$$v_{in2} = -\frac{v_{id}}{2} + v_{ic}$$

$\Rightarrow$ Exact $A_{\text{cm}}$ and $A_{\text{dm}}$ can be solved.

$$A_{\text{dm}} \approx \frac{g_{mi}}{g_{dl} + g_{di}}$$

$$A_{\text{cm}} \approx \frac{-g_o g_{dl}}{2g_{ml} (g_{dl} + g_{di})}$$

$$\text{CMRR} \equiv \left| \frac{A_{\text{dm}}}{A_{\text{cm}}} \right| = 2 \frac{g_{mi} g_{ml}}{g_o g_{di}}$$

Output resistance $r_o \approx \frac{1}{g_{dl} + g_{di}}$

* Longer channel in $M_s$ leads to smaller $g_o$ and higher CMRR.

* $A_{\text{dm}} \propto \frac{1}{\sqrt{I_o}}$ or $(I_o)^{-1/m}$ $\Rightarrow$ higher bias current, lower gain.

* In the weak inversion region, $g_{mi} \propto I_o \Rightarrow A_{\text{dm}} \propto \text{constant}.$

* Cascode current source can be used for $I_o$ to increase CMRR, but $V_{\text{cm}} \downarrow$
* This circuit is not a pure symmetric differential circuit. But it can be approximated by a differential circuit and half-circuit analysis method can be used.

* Signal paths:

\( v_{in1} \rightarrow v_{gsl} : \quad A_v = -g_{mi} \frac{1}{g_{ml}} \)

\( v_{gsl} \rightarrow v_o : \quad A_v = -g_{mi} \left( \frac{r_{ds1}}{r_{ds1}} \right) \)

\( \Rightarrow A_v \bigg|_{v_{in1}} = A_v A_v = g_{mi} \left( \frac{r_{ds1}}{r_{ds1}} \right) = A_{dm} \)

How about \( v_{in1} \rightarrow v_1 \rightarrow v_o \)?

\( v_{in2} : \quad v_{in2} \rightarrow v_o : \quad A_v \bigg|_{vin2} = -g_{mi} \left( \frac{r_{ds1}}{r_{ds1}} \right) = |A_{dm}| \)

How about \( v_{in2} \rightarrow v_1 \rightarrow v_{gsl} \rightarrow v_o \)?

The voltage gain of the four signal paths have nearly the same amplitudes. But different signal paths affect the high frequency response.

Version II: PMOS input

* Lower noise(1/f noise) due to input PMOSs
* Lower output dc voltage

14. The available amplifier circuits in CMOS technology

1). NMOS amplifier in 4-1.1
2). PMOS amplifier with the same configurations as in 4-1.1
3). CMOS amplifiers (NMOS version) in 4-1.2
4). PMOS version with the same configurations as in 4-1.2
Comparisons:
1) NMOS(PMOS) amplifiers versus CMOS amplifiers

<table>
<thead>
<tr>
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<th>single-type MOS amplifier</th>
<th>CMOS amplifier</th>
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<td>Voltage gain</td>
<td>Low</td>
<td>High</td>
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<tr>
<td>Output resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Immunity to process</td>
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<tr>
<td>variations</td>
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<tr>
<td>Power dissipation</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

2) NMOS amplifier (CMOS amplifier with NMOS version) versus PMOS amplifier
   (CMOS amplifier with PMOS version)
   1. Better frequency response
   2. Smaller chip area

3) Differential amplifier versus single-ended-output amplifier
   1. Excellent common-mode signal rejection capability
      Common-mode signals: external noise, dc voltage due to variations, power-supply noise, substrate noise.
   2. Good for weak signal amplification in noisy environment.
   3. Wide applications especially in high-frequency ICs.
   4. More component used ➔ Higher power dissipation and larger chip area.
   5. Matched devices are required ➔ Special care is need in layout and process.
   6. I/O testing requires special I/O external circuits or equipment.

§4.2 Passive-Load MOS Amplifiers
§4-2.1 Resistive-load MOS amplifiers
1. Resistive-Load MOS amplifier
   \[ \text{Av} = -g_{m1}R, \quad r_o \approx R \]
   * Low voltage gain and low \( r_o \)
   * If \( R \uparrow \), M1 might be in the linear region.
   * Only used for low-gain high-frequency amplifier.
     * Parasitic capacitance of \( R \) is smaller than that of the current-source active load.
   * Process variations of \( R \) might be \( \pm 20\% \).
2. Resistive-load MOS phase splitter

\[ A_{v1} \equiv \frac{V_{o1}}{V_i} \equiv -\alpha \frac{R_1}{R_2} \]
\[ A_{v2} \equiv \frac{V_{o2}}{V_i} \equiv -\alpha \frac{g_{m1} R_2}{g_{m1} R_2 + \alpha_i} \]
\[ r_{o1} \equiv R_1 \]
\[ r_{o2} \equiv R_2 \left( \frac{1}{g_m} \right) \]

* R1 and R2 can be chosen so that \( A_{v1} = A_{v2} \)

→ Phase splitter

* Process variation effect of R1 and R2 on \( A_{v1} \) and \( A_{v2} \) is reduced.

3. Resistive-load differential amplifier

* Suitable for low-gain low-\( r_o \) high-frequency amplifiers.

* \( I_{ss} \) can be generated by the constant-gm current source with \( R_{cogn} \)

→ \( I_{ss} \) or \( g_{m1}, g_{m2} \propto \frac{1}{R_{cogn}} \)

→ \( A_{dm} = -g_{m1}R \propto \frac{R}{R_{cogn}} \)

→ Process variation of R and temperature coefficient of R can be compensated.

§ 4-2.2 Inductive load MOS amplifier

1. LC-tank MOS amplifier

* If L is implemented by on-chip inductor, only ~GHz RF operation is allowed.

* L combined with the parasitic capacitance \( C_p \) and the capacitor \( C \) to form a LC tank.

→ Narrow-band amplifier or tuned amplifier.

→ Bandpass amplifier with frequency selectivity.
2. LC-tank MOS cascode amplifier
   * The output LC-tank impedance has a much smaller effect on the input impedance at high frequency due to the isolation effect of M2.

   \[ V_{ODC} = V_{DD} \]
   \[ v_o > V_{DD} \]

3. MOS differential cascode amplifier with series LC-tank
   * \( V_{01DC} = V_{02DC} = V_{DD} \)
   * Two LC-tanks are required.

4. MOS differential cascode amplifier with parallel LC-tank
   * Only one LC-tank is used
     \( \Rightarrow \) chip area ↓
   * \( V_{01DC} = V_{02DC} < V_{DD} \)
   * Bandpass amplifier with the maximum differential gain the same as that of the cascode amplifier.
§ 4-3 Level shifting circuits

Purpose: to provide a dc voltage difference between input and output signals so that the dc level of the output signal is acceptable for the next amplifier stage.

:: At low frequency operation below several tens MHz, dc blocking capacitors are not effective in blocking the dc voltage and passing the ac signal.

DC blocking capacitor:

\[
\begin{array}{c}
\text{v}_i \\
\text{C}
\end{array}
\begin{array}{c}
\text{R} \\
\text{v}_o
\end{array}
\]

ac gain: \[\frac{\text{V}_o}{\text{V}_i} = \left| \frac{R}{R - j \frac{1}{\omega C}} \right| = \frac{R}{\sqrt{R^2 + \left( \frac{1}{\omega C} \right)^2}} \cong \frac{1}{1 + \frac{1}{2} \left( \frac{1}{\omega C} \right)^2} \]

At 10MHz, \( w \cong 6.3 \times 10^7 \) rad/sec

CASE1: If \( C=10\text{PF} \), \( \frac{1}{\omega C} = \frac{1}{6.3} \times 10^4 \Omega \cong 1.6\Omega \)

To obtain 1% signal attenuation, we have

\[ \left| \frac{\text{v}_o}{\text{v}_i} \right| = 0.99 \implies \frac{1}{2} \left( \frac{1}{\omega C} \right)^2 \cong 0.1 \]

\[ \implies R = \left( \frac{1}{\omega C} \right) \frac{1}{\sqrt{0.02}} \cong 11.2\Omega \]

The values of \( R \) and \( C \) are too large and area-consuming.

CASE 2: At 1GHz, \( w=6.3 \times 10^9 \) rad/sec

If \( C=1\text{PF} \), \( \frac{1}{\omega C} = \frac{100}{6.3} \cong 160\Omega \)

The required \( R \) for 1% attenuation is

\[ R = 7 \left( \frac{1}{\omega C} \right) = 1.12\Omega \]

The values of \( R \) and \( C \) are reasonable.
1. Simple level shifting circuit

\[ \Delta V_{DC} = V_{GS} \]

* W/L << 1 to obtain a large \( \Delta V_{DC} \)

* Output resistance looking into Vout

\[ r_o \approx \frac{1}{g_m} \]

\[ \therefore W/L << 1, \quad g_m \downarrow \Rightarrow r_o \uparrow \]

* Frequency response could be degraded by such a large \( r_o \).

\[ \therefore r_o \text{Cout} \uparrow \]

2. High-Z level shifting circuit

\[ \Delta V_{DC} \text{(NMOS)} = + V_{GS} \]

\[ \Delta V_{DC} \text{(PMOS)} = - V_{GS} \]

* \( r_o \approx \frac{1}{g_m} \)

\[ \therefore W/L << 1 \]

\[ \Rightarrow r_o \uparrow (\Delta V_{DC} \uparrow) \]

Frequency response could be degraded.

3. Low-Z level shifting circuit

\[ V^* = V_{TH2} + V_{GS1} \]

\[ = V_{TH2} + V_{TH1} + \left[ \frac{I_x}{\left( \frac{\mu C_{ox}}{W/L} \right) (W/L)} \right] \]

\[ \text{Cout} \]

\[ r_o \]

\[ -V_{SS} \]
\[ V_1 = V^* + \frac{I_1}{\sqrt{\left(\frac{\mu C_{\text{ox}}}{2}\right)(W/L)_2}} \]

\( (W/L)_1 << 1 \) and \( (W/L)_2 >> 1 \) \( \Rightarrow \) large enough \( V^* \)

\[ V_1 \equiv V^* \text{ independent of } I_1 \]

* \( V_1 \) (dc voltage shift) can be stabilized by choosing a large \( (W/L)_2 \) and a stable \( I_x \).

* \( r_0 \equiv \frac{1}{g_{m_2}} \) is not large since \( (W/L)_2 >> 1 \).

\( \Rightarrow \) Better frequency response.

4. Replica bias circuit

\( (W/L)_6, (W/L)_4 >> 1 \)

\[ \Rightarrow V_{GS4} \equiv V_{GS6} \equiv V_{THN} \]

\[ V_X \equiv V^* \]

\[ V_{BIAS} \]

\( (W/L)_2, (W/L)_3 >> 1 \)

\[ \Rightarrow V_{GS2} \equiv V_{GS2A} \equiv |V_{THP}| \]

\[ V_2 \equiv V_{2A} \]

\( M_1 \equiv M_{1A} \) and \( M_3 \equiv M_5 \)

\[ I_{DS3} = I_{DS5} = I_X \]

\[ V_{GSI} = V_{GS1A} \]

\[ V_{BIAS} = V_{GS1} + V_2 = V_{GS1A} + V_{2A} = V_y \]

* Provide a fixed bias voltage \( V_y = V_{BIAS} \) at the input node to stabilize the preceding stage.

* Provide a DC voltage shift of \( V_Y - V_X^* \).

* The output resistance looking into the OUT node is very small

\[ (r_o \equiv \frac{1}{g_{m_{2A}}} || \frac{1}{g_{m_6}}), (W/L)_2, (W/L)_6 >> 1 \Rightarrow r_o \downarrow \]

* The matching between \( M_1(M_3) \) and \( M_{1A}(M_5) \) is very important to stabilize \( V_Y \).

\[ \S \ 4-4\text{ MOS Output stages} \]

\[ \S \ 4-4.1\text{ Requirements} \]
(1) Suitable power and voltage swing to drive an adequate external load equally in both positive and negative directions.
(2) Acceptably low levels of signal distortion.
(3) Minimum output impedance.
(4) Low quiescent power dissipation and maximum efficiency.
(5) High frequency response.
(6) Buffering the previous gain stage from $C_L$ or $R_L$

§ 4-4.2 NMOS (PMOS) Output Stages

1. Source followers (Enhancement device)
   * Voltage swing:
     \[ v_{\text{o max}}^+ = V_1 - V_{\text{GS}} \]
     \[ = V_{\text{DD}} - V_{\text{TH}} - V_{\text{GS}} \text{ (or } V_{\text{TH1}}) \text{ (not full level to } V_{\text{DD}}) \]
     \[ v_{\text{o max}}^- = V_{\text{BIAS}} - V_{\text{TH}} \text{ (} M_2 \text{ sat)} \]
     \[ = -V_{\text{SS}} \text{ (} M_1 \text{ off)} \]
   * $r_0 \equiv \frac{1}{g_{m1}}$
     Small $r_0$ Need large $(W/L)_1$ and $I_{DS1}$
     * The rise time is decreased by the larger $(W/L)_1$
       But the fall time is fixed by $I_{DS2}$
       =>Unsymmetric driving capability.
   * Provide a dc voltage shift and a voltage gain smaller than 1

2. Phase-splitting output driver
   * Voltage swing: (low)
     \[ v_{\text{o max}}^+ = V_{\text{DD}} - V_{\text{TH}} - V_{\text{TH5}} \]
     (M2 and M4 are off)
     \[ v_{\text{o max}}^- = -V_{\text{SS}} - V_{\text{GS}} + V_{\text{TH}} \text{ (M4 sat.)} \]
     \[ = -V_{\text{SS}} + V_{\text{DS}} > -V_{\text{SS}} \]
     (maximum)
   * Fall time is not limited by the current source.
   * $r_0 \approx \left( \frac{1}{g_{m5}} \right) (r_{ds4}) \approx \frac{1}{g_{m5}}$
3. NMOS output stage with feedback

M3, M4 : output common-source amplifier.
M1, M2 : First common-source amplifier
M2 : series-shunt negative feedback
Series-shunt negative feedback
=> voltage gain ↓
frequency bandwidth ↑
output resistance ↓

\[
 r_o = \frac{\alpha_4}{1 + \left( \frac{\alpha_2 \alpha_4 g_{m3}}{g_{m4}} \right)} \\
\text{midfrequency output resistance}
\]

\[
 A_v = \frac{g_{m1}}{g_{m2}} \frac{\alpha_2 \alpha_4 g_{m3}}{g_{m4}} \left( 1 + \frac{\alpha_2 \alpha_4 g_{m3}}{g_{m4}} \right) \\
\text{midfrequency voltage gain}
\]

\[
 A_v \approx \left[ \frac{\sqrt{W/L}}{\sqrt{W/L}} \right] \frac{\sqrt{W/L}}{\sqrt{W/L}} \frac{\sqrt{W/L}}{\sqrt{W/L}} \\
\text{If } \alpha \to 1
\]

* Larger \( \frac{g_{m3}}{g_{m4}} \) \( \Rightarrow r_o \downarrow \), \( A_o \uparrow \)

* The W/L ratio of M1,M2,M3 and M4 can be suitably designed to satisfy the specifications on (1) voltage gain ; (2) output swing ; (3) power dissipation ; (4) chip area ; (5) fast transient ; (6) good frequency response. ((5) and (6) involve non-linear analysis )
§ 4-4.3 CMOS Output Stages

1. Simple source follower (NMOS and PMOS)
   Too larger \( r_o \)

2. Class AB puah-pull CMOS output buffer
   * Capable of low standby power.
     e.g. \( I_{\text{bias}} \cong nA \)
     \( I_{\text{out}} \cong < 1mA \)
   * \( V_{\text{ODC}} = \frac{V_{DD} + V_{SS}}{2} \) is desired

* Small output voltage swing.
  If \( R_i \) exists at the output node, the voltage swing is further degraded.

3. Emitter-follower output stage.
   * \( r_o \downarrow \)
   * \( Q_i \) : free BJT in CMOS n-well technology.
   Voltage swing:
   \[ V_{O\text{max}}^- = v_i + |V_{BE}| \]
   \[ = V_{SS} + |V_{BE}| \quad (\text{if } \quad v_{i\text{max}}^- = -V_{SS}) \]
   \[ V_{O\text{max}}^+ = +V_{DD} \quad (\text{If } \quad Q_i \text{ is off}) \]

* The collector series resistance \( r_c \) of \( Q_i \) may degrade the output swing and saturate the transistor.
Chapter 5 Midband Analysis of CMOS Operational Amplifiers (OP AMPS)

§5-1 General Considerations

§5-1.1 General Procedures to analyze an OP AMP IC

1. Identify all the biasing circuits (current & voltage).
2. Identify all the protection circuits and then take them away.
3. Calculate all the operating currents and voltages.
4. Trace the signal path and identify the amplifier, buffer, level shifter, and output driver configurations.
5. Calculate the midfrequency gain.
6. Identify the compensation circuits.
7. Calculate the high-frequency response.
8. Perform the SPICE simulations to obtain the performance parameters.

§5-1.2 Some important OP AMP Specifications

1. Open-loop differential gain $A_d(\omega)$.
2. Open-loop common-mode gain $A_c(\omega)$.
3. Common-mode rejection ratio (CMRR)

$$CMRR(\omega) \equiv \left| \frac{A_d(\omega)}{A_c(\omega)} \right| = \left| \frac{\partial V_{ic}}{\partial V_{io}} \right|_{V_{io}=0}^{-1}$$

where $V_{io}$ is the input offset voltage

$V_{ic}$ is the input common-mode voltage
4. Output swing.
5. Unity-gain frequency \( f_u \).

6. Upper 3-dB frequency \( f_{3.1dB} \).

7. Power-supply rejection ratio (PSRR).

\[
PSRR' (\omega) \equiv \left| \frac{A_i(\omega)}{\frac{\partial V_n}{\partial V_{DD}}} (\omega) \right| = \left[ \frac{\partial V_{i_{in}}}{\partial V_{DD}} (\omega) \bigg|_{V_{i}=0} \right]^{-1}
\]

\[
PSRR (\omega) \equiv \left| \frac{A_i(\omega)}{\frac{\partial V_n}{\partial V_{SS}}} (\omega) \right| = \left[ \frac{\partial V_{i_{in}}}{\partial V_{SS}} (\omega) \bigg|_{V_{i}=0} \right]^{-1}
\]

8. Slew rate and settling time

Slew rate: Maximum \( \frac{d}{dt} V_o \) in an unity-gain close-loop OP Amp with a fixed step input under maximum load.

Settling time: The time required for the OP AMP in an unity-gain closed loop to reach \( \sim \% \) of its final value with a fixed step input under maximum load.

9. Linearity and harmonic distortion

Usually dominated by the output stage.

Closed-loop characteristics.

10. Equivalent input noise and input offset

Usually dominated by the input stage.

§5-1.3  General Block Diagram of an OP AMP

[Diagram showing the block diagram of an OP AMP with stages labeled as Input Stage, Buffer or Level Shifter, Gain Stage, Buffer or Level Shifter, and Output Driver Stage.]

differential-input-to-single-end-output converter

to provide high gain

to provide small \( r_o \) or to drive large \( C_L \) or small \( R_L \)
§5-2 One-Stage (Single-Stage) CMOS OP AMPS

§5-2.1 Single-ended-output OP AMPS

1. Simple OP AMP
   * Inverting input: 2
   * Noninverting input: 1
   * Open-loop voltage gain

\[ \frac{v_o}{v_i} = A_d = -g_{mN} \left( \frac{r_{dsP}}{r_{dsN}} \right) \]

* Open-loop output resistance

\[ r_o = r_{dsP} // r_{dsN} \]

Close-loop output resistance

\[ r_{oc} \simeq \frac{r_{dsP} // r_{dsN}}{1 + g_{mb} \left( \frac{r_{dsP}}{r_{dsN}} \right)} \simeq \frac{I}{g_{mN}} \]

The closed-loop output resistance is independent of the open-loop output resistance.

* The dominate pole is located at the output with the RC time constant \( r_o C_L \).

* \( A_d \sim 100 \), Power dissipation \( \sim \mu W \), \( f_o \sim \text{MHz} \).
   Suitable for small-load internal-use applications.
* Cannot drive heavy load.

* Output swing: \( V_{DD} - |V_{DSAT5}| \rightarrow -V_{SS} + V_S + V_{DSAT4} \)

2. Telescopic cascode OP AMP with cascode-current-source load

* Open-loop voltage gain

\[
A_d = -g_{mN} \left( g_{mB} r^2_{dsN} // g_{mP} r^2_{dsP} \right)
\]

* Open-loop

\[
r_o = g_{mN} r^2_{dsN} // g_{mP} r^2_{dsP}
\]

Close-loop

\[
r_{oc} = \frac{1}{g_{mN}}
\]

* In the unity-gain feedback, the node 2 is connected to the output node.

\[\Rightarrow M_2 \text{ and } M_4 \text{ sat.} \]

\[\Rightarrow V_{o\min} = V_{BIAS} - V_{TH4}, \]

\[V_{o\max} = V_x + V_{TH2} = V_{BIAS} - V_{GS4} + V_{TH2}\]

\[\Rightarrow \text{Output swing} = V_{TH2} - (V_{GS4} - V_{TH4}) \leq V_{TH2}\]

Too small output swing

Not suitable for unity gain buffer.

* Limit output swing:

\[V_{DD} - |V_{DSAT5}| - |V_{DSAT6}| \rightarrow -V_{SS} + V_S + V_{DSAT2} + V_{DSAT4}\]

3. Telescopic cascode OP AMP with high-swing cascode-current-source load
* Higher output swing
* Not suitable for unity-gain buffer

4. Telescopic cascode OP AMP with gain-boosting (or enhanced-output-impedance) circuit

1) Basic concept

* \( v_i \rightarrow Av_i \rightarrow i_o = Ag_m v_i \)

\[ \frac{i_o}{v_i} = Ag_m \]

The transconductance is boosted by \( A \) times, \( A \sim 100 \).

* \( r_i \approx \frac{l}{g_m A} \sim 100\Omega - 10\Omega \)

The input resistance is lowered by \( A \) times.
Suitable for current input because of small \( r_i \).
\( \Rightarrow \) High injection efficiency
Example:

If the output resistance of $D$ is not large, e.g. $r_D = 10K\Omega$,

We need $r_i \leq 100\Omega$ to obtain $I_i = I_L \frac{10K\Omega}{10K\Omega + r_i} \approx 99\%$ of $I_L$

$\Rightarrow 99\%$ injection efficiency and stable photodiode reverse bias $V_{\text{BIAS}}$

* $r_o \equiv (G_{m2} r_{d1}) r_{d2} = A r_{d1} r_{d2}$

The output resistance is boosted by $A$ times as compared to the cascode structure without $A$.

No extra cascode device is required

$\Rightarrow$ The swing is not further degraded.

* Offset voltage problem

$A = 100, V_{OS} = 0V, V_{GS5} = 1.4V > V_{TH5} = 1.1V,$

$\Rightarrow v_i = 14mV$ and $M_5$ is turned on to provide negative feedback.
But if $V_{OS} = -5$ mV

$\Rightarrow V_{GS5} = 0.9$ V smaller than $V_{THS}$

$\Rightarrow M_5$ is off and the circuit fails.

So suitable systematic offset should be introduced to make sure that $V_{OS} > 0$

* Realization

2) Current mirror with enhanced-output-impedance circuit

A: The Sackinger implementation
* Low swing

\[ r_o = (g_{m4} r_{ds2} r_{ds1}) [g_{m6} (r_{ds6} / r_{os2})] \]

* Minimum required \( V_{\text{out}} \)

\[ V_{\text{out}} = V_{GS6} + V_{GS4} - V_{TH4} \]

* \( V_{GS6} = V_{GS5} \Rightarrow V_{DS1} = V_{DS2} \) precise current ratio

B: High-swing implementation

* Add extra devices \( M_7 \) and \( M_8 \) to decrease \( V_{DS1} \) and \( V_{DS2} \).

* \( V_{DS1} = V_{GS5} - V_{GS7} \)
\( V_{DS2} = V_{GS6} - V_{GS8} \)

* High swing

Min \( V_{\text{out}} = V_{GS6} - V_{GS8} + V_{GS4} - V_{TH4} \)

* \( I_{\text{out}} = K I_{\text{REF}} \)

\( V_{DS1} = V_{DS2} \Rightarrow \) precise ratio

3) OP AMPS

A: Using the gain-boosting circuit in cascode amplifier

* \( g_{m3} = g_{m4} \) is increased by \( A \) times.

* The effective resistance seen by \( M_1 \) and \( M_2 \) is lowered by \( A \) times

\( \Rightarrow \) The gain is lowered by \( A \)
times.

⇒ Has much less Miller capacitance at the input while keeping $M_1$ and $M_2$ saturated.

* $r_o$ seen by $M_3$ and $M_4$ is increased by $A$ times ⇒ Gain boosting

* Realization

Why $I_{SS2}$?

The amplifier $A$ is realized by fully differential folded cascode amplifier
B: Using the gain-boosting circuits in both cascode amplifier and current-mirror load

5. Folded cascode OP AMP

1) PMOS input

* Higher power dissipation than the telescopic cascode OP AMP.
* Higher input equivalent noise and input offset voltage
  :: More devices are involved.
* Higher $V_{ICM}$ range and higher output swing.
* Lower voltage gain as compared with the PMOS-input telescopic cascode OP AMP. Why?
* Lower $r_o$

2) With the gain-boosting circuit

§5-2.2 Fully differential OP AMPs

1. Simple OP AMPs

* $A_{dn} \equiv -g_{mN}(r_{dSN} / / r_{dSP})$
\[ A_{_\text{cm}} = -\frac{\alpha_r r_{_\text{dp}}}{2r_o} \]

\[ \text{CMRR} = \frac{\alpha_r g_{_mN}(r_{_\text{dp}} // r_{_\text{dp}})}{2r_o} \]

* Power supply noise gain

\[ A_{_\text{vddm}} \equiv +g_{_mP}[r_{_\text{dp}} // (g_{_mN} 2r_o)]\left[ \frac{1}{g_{_mP} r_{_\text{REF}} + 1} \right] \equiv \frac{r_{_\text{dp}}}{r_{_\text{REF}}} \equiv 1 \]

\[ A_{_\text{vcom}} \equiv + \left( \frac{g_{_mN}}{2r_o + \frac{1}{g_{_mN}}} \right)[g_{_mN} (r_{_\text{dp}} // r_{_\text{dp}})] = \frac{r_{_\text{dp}}}{2r_o + \frac{1}{g_{_mN}}} \]

\[ PSRR^+ \equiv \left| \frac{A_{_\text{dm}}}{A_{_\text{vddm}}} \right| = \frac{g_{_mN} (r_{_\text{dp}} // r_{_\text{dp}})}{g_{_mP} r_{_\text{dp}}} \]

\[ g_{_mP} > g_{_mN} \quad \text{for large} \; PSRR^+ \]

\[ PSRR^- \equiv \left| \frac{A_{_\text{dm}}}{A_{_\text{vcom}}} \right| = \frac{g_{_mN} (r_{_\text{dp}} // r_{_\text{dp}})(2r_o + \frac{1}{g_{_mN}})}{(r_{_\text{dp}} // r_{_\text{dp}})} \equiv 2g_{_mN}r_o \]

\[ PSRR^- > PSRR^+ \]

* Common-Mode Feedback (CMFB) is required to decrease \( A_{_\text{cm}} \) and increase CMRR. With CMFB circuit, \( PSRR \uparrow \).

2. Telescopic cascode OP AMPs with cascode or high-swing cascode current-source load
3. Telescopic cascode OP AMPS with gain-boosting cascode amplifier or current-source load
   * To obtain maximum swings at the output, \( A_2 \) must employ an NMOS-input differential pair (high output dc voltage) whereas \( A_1 \) an PMOS-input one (Low output dc voltage)
   * Very high voltage gain
4. Folded cascode OP AMPS with cascode, high-swing cascode, or gain-boosting current-source load

\[ \text{Diagram of OP AMP circuit} \]

§5-3 General-Purpose Two-Stage CMOS OP AMPS

§5-3.1 Single-ended-output OP AMPS

1. PMOS-input design I

\[ \text{Diagram of PMOS-input design I} \]

\[ M_{10}, M_1 : \text{Master stage of PMOS current mirror.} \]

\[ M_5, M_6, M_9 : \text{Slave stages} \]

\[ M_1, M_2, M_3, M_4, M_5 : \text{Differential-input-to-single-ended output converter (input stage)} \]

\[ M_8, M_9 : \text{CS amplifier with current-source load (gain stage)} \]
$M_6$, $M_7$, $C_C$ : Compensation circuit with source follower.

OP AMP Characteristics :

Open-loop dc gain: 60 ~ 66 dB

CMRR : 60 dB

2. PMOS-input design II

![PMOS-input design II diagram]

$C_C$ : Compensation capacitor

$R$ : n+ diffusion resistor

* First commercial CMOS OP AMP

* Designed by Motorola in 12-bit ADC.

3. NMOS-input design with level-shifted CMOS amplifier

![NMOS-input design with level-shifted CMOS amplifier diagram]

$C_2$ : for PSRR ($V_{DD}$) consideration.

$C_I$ : normal compensation capacitor

* Designed by AMI in PCM voice CODEC.

OP AMP characteristics:

- Open-loop gain: 90 dB
- CMRR: 73 dB
- PSRR+: 68 dB
- PSRR-: 70 dB
- Input offset: 10 mV (standard deviation)
- Input offset: 0.4 mV (mean)

4. Typical characteristics of CMOS 2-stage OP AMPS


- Open-loop dc gain ($C_\text{l}$ only): $10^3 \sim 10^4$ (60 dB ~ 80 dB)
- PSRR: 60 dB ~ 70 dB
- Input offset: 2 mV (standard deviation)
- Input common-mode range: within 1V of supply voltage.

5. Output Transconductance Amplifier (OTA) or current-mirror OP AMP

\( M_3, M_5 / M_4, M_6 \) : PMOS current mirrors
\( M_7, M_8 \) : NMOS current mirror
\( M_1 \sim M_4, M_5 \) : Input stage
\( M_5 \sim M_8 \) : Gain stage

\[ \Delta V_{in} \text{ (input differential voltage)} \Rightarrow \Delta I \Rightarrow K \Delta I \Rightarrow \Delta I_{out} = \]
\[ 2K \Delta I = I_o \]

\[ G_m = \frac{\Delta I_{out}}{\Delta V_{in}} = g_m K \quad A_v = G_m \left( r_{ds6} // r_{ds8} \right) \]

Characteristics:
Open-loop gain : 58 dB
Total dc current : 4\( \mu \)A
Output load capacitance : \( \sim 10pF \)

* DC power dissipation can be decreased.
  Micropower ICs for low-power applications.
* Frequency response, slew rate, and output load \( C_L \) are limited.

6. Modified OTA

\[ +V_{DD} \]
\[ -V_{SS} \]
\[ M_5 \]
\[ M_6 \]
\[ M_7 \]
\[ M_8 \]
\[ V_{BIAS} \]
\[ M_1 \]
\[ M_2 \]
\[ M_3 \]
\[ M_4 \]
\[ V_o \]
\[ I_{SS} \]
Higher \( G_m \) and higher open-loop voltage gain.

\[
G_m \equiv 2g_m_{12} (r_{ds_{34}} \parallel r_{ds_{12}}) \ g_m_{56}
\]

* Frequency compensation is required.
* Designed by Toshiba in C\(^2\)MOS ADC.

* \( M_5 \ (M_7 \) is matched to \( M_6 \ (M_8 \) \)

=> The effect of \( V_{TH} \) variations on \( M_6 \) and \( M_8 \) can be reduced.

§ 5-3.2 Fully differential OP AMPS

1. Simple OP AMP

* Open-loop gain \( A_v \equiv g_m_{12} (r_{ds_{12}} \parallel r_{ds_{34}}) \ g_m_{56} (r_{ds_{56}} \parallel r_{ds_{78}}) \)
* Frequency compensation is required.
* CMFB is required.
2. High-gain OP AMP

![High-gain OP AMP diagram]

* Higher gain because of high-swing cascode current-source load.

* If high-swing cascode current source is not used, the design of $M_9$ and $M_{10}$ is difficult.

\[
\therefore V_{GS910} = V_{DS78} + V_{DS56}
\]

3. General comparison

<table>
<thead>
<tr>
<th></th>
<th>Gain</th>
<th>Output Swing</th>
<th>Power Dissipation</th>
<th>Speed</th>
<th>Noise</th>
</tr>
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<td>Telescopic</td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
<td>Highest</td>
<td>Low</td>
</tr>
<tr>
<td>Folded Cascode</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
</tr>
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<td>Two-stage</td>
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<td>Highest</td>
<td>Medium</td>
<td>Low</td>
<td>Lowest</td>
</tr>
<tr>
<td>Gain-boosted</td>
<td>High</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
</tr>
</tbody>
</table>
§ 5-4 General-Purpose Three-Stage CMOS OP AMPS

1. Using the emitter follower as output stage

\[ I \]

\[ +V_{DD} \]

\[ -V_{SS} \]

\[ M_6, M_9, C_C \]: Frequency compensation circuit

\[ Q_2 \]: Protection circuit for \( Q_1 \) to avoid the reverse breakdown of B-E junction diode of \( Q_1 \).

\[ Q_1, M_{10} \]: Emitter follower as output stage.

* Designed by Westinghouse for analog signal processing.

* Open-loop gain = 60db, power dissipation = 16mW.
II.

M10, M11, C1: Frequency compensation circuit.
C2, C3: Improving frequency response of Av and PSRR.

§5-5 Common-Mode Feedback (CMFB) Circuits

Purposes: 1. To provide a stable common-mode level to the nodes.
2. To decrease the common-mode gain.

Design Considerations:

1. To create a negative feedback path only for common-mode signals. For differential signals, CMFB has no effect on circuit performance.
2. To keep power dissipation and chip area of CMFB circuit as low as possible.
3. CMFB is not required in single-ended-output OP amps. But it can be used to boost CMRR.
4. CMFB is required in differential-output OP amps.
§5-1.1 CMFB circuits for single-ended-output CMOS OP AMPs


M₈, M₉, M₁₀, M₁₁ : CMFB circuit

\[ M₉ ≡ M₁₀ ≡ M₄ ≡ M₅ \]

* IN+, IN- ↑ ⇒ X, Y ↑ ⇒ common-mode voltage ↑
  IN+, IN- ↑ ⇒ B ↑ ⇒ C ↑ ⇒ X, Y ↓ ⇒ compensation

* For differential signals, A and B are ac grounded
  ⇒ CMFB circuit has no effect on differential signals.

* What is the purpose of M₈?

* Designed by Toshiba in C²MOS ADC

* OP AMP characteristics:
  Supply voltage : 5V
  Supply current : 150μA
  Input common-mode range : +1V ~ +4.5V
  Input offset voltage : ± 1mV
  CMRR : 75dB
  Open-loop gain : 90dB
  Output swing : 0 ~ 5V

$+$ $V_{DD}$

Q₁, I₂, Cₓ : Frequency compensation circuit
M₆, M₇, M₈, M₉, M₁₀ : CMFB circuit.

* IN⁺, IN⁻  $\uparrow$  $\Rightarrow$  X, Y  $\downarrow$  $\Rightarrow$  common – mode voltage $\downarrow$

  $\Rightarrow$  A  $\uparrow$  $\Rightarrow$  B  $\downarrow$  $\Rightarrow$  X, Y  $\uparrow$  $\Rightarrow$ compensation.

* For differential signals, A is ac grounded.
  $\Rightarrow$ No effect on differential signals.

* Keep $I_{DS6}=I_{DS7}=25$  $\quad$  $I_{DS9}=I_{DS8}=I_{DS5}=50$
  and $I_{DS3}=I_{DS4}=25$

* Designed by MOSTEK in PCM Codec.
5-5.2 CMFB circuit for differential-output CMOS OP


MN3, MN3A: CMFB circuit

*Common-mode signals at $X,Y \uparrow \Rightarrow A \downarrow \Rightarrow B,C \downarrow \Rightarrow X,Y \downarrow$

*For differential signals, A is ac grounded.
*Why MN4 and MN4A?
*Output swing is decreased by MN3 and MN3A.
   To reduce the effect, MN3 and MN3A can be operated in the linear region.
*Output CM level is still a function of device parameters.

*Under differential signals, due to $I_{DS}$ nonlinearity, A is not exactly ac ground $\Rightarrow$ differential characteristics are changed.

M13–M20: CMFB circuit

Cascoded common-mode amplifier

*For differential signals, nodes A, B, and C are ac grounded.
3. Resistive CMFB circuit

* For differential signals, A is ac grounded.

\[ A_{dm} = g_{m12} \left( \frac{r_{ds12}}{r_{ds14}} / \frac{1}{R_F} \right) \]

\[ A_{dm} \text{ is decreased by } R_F \]

* For CM signals,

\[ A_{cm} = -\alpha_{12} \frac{1}{2g_{m34}r_o} \]

smaller than \( -\frac{\alpha_{12}}{2r_o} \left( \frac{r_{ds34}}{g_{m12}r_{ds12}r_o} \right) \)

\[ \Rightarrow \text{CMRR} \uparrow \]

4. Dynamic CMFB (DCMFB) circuit


\( V_{CMO}, \; \phi_1, \; \phi_2, \; M_a \sim M_b \) : CMFB circuit

\( M_1 \sim M_6 \) : current sources associated with CMFB circuit

* DCMFB versus static CMFB

1. Less power dissipation.
2. Has no effect on output swing, noise, and speed of the OP AMP.
3. \( \phi_1, \; \phi_2 \) nonoverlapping clocks are required.
§6-1 Single-Stage Amplifier

§6-1.1 Source follower

A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{sC_{gs1} + g_{m1}}{R_s(C_{gs1}C_{Leq} + C_{gs1}C_{gd1} + C_{gd1}C_{Leq})s^2 + \left(\frac{g_{m1}}{\alpha_1}R_sC_{gd1} + C_{Leq} + C_{gs1}\right)s + g_{m1} / \alpha_1 + G_{Leq}}

where \( G_{Leq} = g_{db1} + g_{db2} \), \( C_{Leq} = C_L + C_{sb1} + C_{dh2} \)

* Left-Half-Plane (LHP) pole: \( f_p = \frac{G_{Leq} + g_{m1} / \alpha_1}{2\pi(C_{gs1} + C_{Leq})} \)

LHP zero: \( f_z = \frac{g_{m1}}{2\pi C_{gs1}} \)

In general, \( f_p < f_z \) \( \Box \) \( C_{Leq} > C_{gs1} \)

* If \( \frac{C_{Leq}}{C_{gs1}} = \left(\frac{1}{\alpha_1} - 1\right) + \frac{G_{Leq}}{g_{m1}} \), we have

\( f_p = f_z \) and \( A_v(s) \equiv \frac{C_{gs1}}{C_{gs1} + C_{Leq}} \approx 1 \) indep. of \( s \).

=> Better high frequency response.

How to achieve this?

Adding an extra capacitor \( C_x \) such that
\[ C_x + C_{gs1} = C_{Leq} \left( \frac{1}{\alpha_i - 1} + \frac{G_{Leq}}{g_{ml}} \right) \]

\[
Z_i(s) \equiv \frac{V_i(s)}{I_i(s)} = \left[ \frac{1}{C_{gs1} s} + \frac{C_{gs1} s + g_{ml}}{C_{gs1} s (G_{Leq} + g_{mb1} + s C_{Leq})} \right] (C_{gd1} s)
\]

* If \( g_{mb1} + G_{Leq} \ll C_{Leq} \) and \( C_{gd1} \) is neglected,

\[
Z_i(s) \approx \frac{1}{C_{gs1} s} + \frac{1}{C_{Leq} s} + \frac{g_{ml}}{C_{gs1} C_{Leq} s^2}
\]

The input impedance consists of the series connected

\( C_{gs1}, C_{Leq} \), and the negative resistance

\[-\frac{g_{ml}}{C_{gs1} C_{Leq} \omega^2}\]

Thus oscillation is possible.

* If \( g_{mb1} + G_{Leq} \) is neglected, the equivalent input capacitances

\[
C_{in} = C_{gd1} \parallel C'_{in}
\]

\[
C_{in}' \equiv C_{Leq} \left( \frac{1}{C_{Leq} s + 1 + \frac{g_{ml}}{C_{gs1} s}} \right)
\]

For large \( g_{m1}, C_{in}' < C_{Leq} \)

The large load capacitance \( C_L \) is well blocked or buffered from the preceding stage.

\[
Z_o(s) \equiv \frac{V_o(s)}{I_o(s)} \bigg|_{V_{in}=0} = \frac{1}{G_{Leq} + g_{mb1} + s C_{Leq} + (s C_{gs1} + g_{ml}) \left( \frac{R_s (C_{gd1} s + 1)}{R_s (C_{gd1} s + C_{gs1} s) + 1} \right)}
\]

* If \( s = 0 \), \( Z_o = R_o = \frac{1}{g_{ml} + g_{mb1}} \)

If \( s \approx \omega \), \( Z_o'(\text{without } C_{Leq}) \approx R_s \) for \( R_s < \frac{1}{G_{Leq} + g_{ml}} \) and \( C_{gs1} \gg C_{gd1} \)

Since usually \( R_s > \frac{1}{g_{ml} + g_{mb1}} \), we have
\[ |Z_0| \alpha \omega = \rightarrow \text{Inductive load} \]

\[ Z_0(s) = \frac{R C_{gds} s + 1}{g_{m1} / \alpha_i + C_{gds} s} \]

\[ R_1 = R_s - \frac{\alpha_i}{g_{m2}} \]

\[ R_2 = \frac{\alpha_i}{g_{m2}} \]

\[ L = \frac{C_{gds} \alpha_i}{g_{m2}} (R_s - \frac{\alpha_i}{g_{m2}}) \]

\[ L \text{ and } C_L \text{ causes output signal ringing.} \]

* Two source followers in cascade might cause oscillation because
  First SF : L in Zo 1
  Second SF : -R and Cin Zo 2

§6-1.2 Enhancement - load NMOS common-source gain stage
Applying the Miller’s theorem, we have

\[ G_{\text{leq}} = g_{ds1} + g_{ds2} + g_{m2} + g_{mb2} \]
\[ C_{\text{leq}} = C_{db1} + C_{gs2} + C_{sb2} + C_L \]

\[ C_{\text{in}} = C_{gs1} + C_{gdl}(1 + g_{m1}/G_{\text{leq}}) \]

\[ = \frac{G_{\text{leq}} (sC_{gdl} - g_{m1})}{(sC_{\text{in}} + G_{\text{leq}})s(C_{\text{leq}} + C_{gdl}) + C_{\text{leq}}} \]

* Right-Half-Plane Zero : \( S_z = g_{m1}/C_{gdl} \)
* Left-Half-Plane Poles : \( S_{p1} = -G/C_{\text{in}} \) (input pole)
  \( S_{p2} = -G_{\text{leq}}/(C_{\text{leq}} + C_{gdl}) \) (output pole).
  If \( C_{gdl} \) and \( C_{\text{leq}} \) are small \( \Rightarrow S_{p1} \) is the dominant pole.
* If \( C_L \) is large, the dominate pole is \( S_{p2} \approx (g_{m2} + g_{mb2})/C_L \)
* The input impedance can be approximated by

\[ Z_{\text{in}} \approx \frac{1}{C_{gdl} + (1 + g_{m1}/G_{\text{leq}})C_{gdl}} \text{ near the upper 3dB frequency.} \]

* The exact \( Z_{\text{in}} \)

\[ Z_{\text{in}} \approx C_{gs1} \left| \frac{1 + \frac{1}{G_{\text{leq}}}(C_{gdl} + C_{\text{leq}})s}{C_{gdl}(1 + g_{m1}/G_{\text{leq}}) + \frac{1}{G_{\text{leq}}}(1 + g_{m1}/G_{\text{leq}})s} \right| \]

If \( \frac{1}{G_{\text{leq}}}(C_{gdl} + C_{\text{leq}})s \ll 1 \) and \( \frac{1}{G_{\text{leq}}}C_{gdl}s \ll (1+g_{m1}/G_{\text{leq}}) \),

\( Z_{\text{in}} \) can be approximated by the previous formula.
§ 6-1.3 Cascode amplifier stage

\[ g_2 = g_{m2} + \frac{1}{r_{ds1}} \]

\[ C_2 = C_{gs1} + (1 + \frac{g_{m1}}{g_{m2}})C_{gd1} \]

\[ C_2 = C_{gd1} + C_{db1} + C_{gs2} + C_{sb2} \]

\[ C_{Leq} = C_1 + C_{gd2} + C_{db2} + C_{sb3} + C_{gs3} \]

\[ A_\chi(s) = \frac{-G_s g_m (sC_{gd1} - g_m)}{(sC_1 + G_s)(sC_2 + g_m)(sC_{Leq} + g_m)} \]

RHP Zero: \( S_z = \frac{g_{m1}}{C_{gd1}} \)

LHP Pole : \( S_{p1} = -\frac{G_s}{C_1} ; S_{p2} = -\frac{g_2}{C_2} ; S_{p3} = -\frac{g_{m3}}{C_{Leq}} \)

\( S_{p1} \) usually is the dominant pole.

\[ \Rightarrow f_{3dB} \approx \left| S_{p1} \right| = \frac{G_s}{2\pi C_1} \]

* Typically, \( g_{m1} = g_{m2} \), then \( C_1 = C_{gs1} + 2C_{gd1} \)
\[ 6 - 6 \]

6-1.4 CMOS gain stage

\[ G_{\text{leq}} = g_{ds1} + g_{ds2} \]

\[ C_{\text{leq}} = C_{db1} + C_{db2} + C_L \]

\[ C_{in} = C_{gs1} + C_{gs2} + (1 + \frac{g_{m1} + g_{m2}}{G_{\text{leq}}})(C_{gd1} + C_{gd2}) \]

\[ A_v(s) = \frac{G_s[s(C_{gd1} + C_{gd2}) - (g_{m1} + g_{m2})]}{[s(C_{gd1} + C_{gd2} + C_{\text{leq}}) + G_{\text{leq}}](sC_{in} + G_s)} \]

RHP Zero: \( S_z = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}} \)

LHP Pole: \( S_{p1} = -\frac{G_s}{C_{in}} \)

\[ S_{p2} = -\frac{G_{\text{leq}}}{C_{gd1} + C_{gd2} + C_{\text{leq}}} \]

If \( R_s \) is large enough (\( R_s \) is the output resistance of the preceding stage),

\[ |S_{p1}| \ll |S_{p2}| \]

\( S_{p1} \) is the dominant pole.
6-1.5 CMOS differential amplifier

1. Differential-mode half circuit

\[
\begin{align*}
\frac{1}{2} V_{id} & \quad C_{gds1} \quad \frac{1}{2} g_{m1} V_{id} \quad C_{Leq} \\
\frac{1}{2} V_{od} & \quad r_{ds1} \quad r_{ds1} \quad + \\
& \quad - \\
C_{Leq} & \equiv C_L + C_{db4} + C_{db1}
\end{align*}
\]

\[+V_{DD} \quad V_{BIAS} \quad M_4 \quad +V_{DD} \quad V_{BIAS1}\]

\[\frac{1}{2} V_{id} \quad M_1 \quad \frac{1}{2} V_{od} \quad -V_{SS} \quad -V_{SS}\]

\[A_d = \frac{V_{od}}{V_{id}} = H(s) = -\frac{g_{m1}}{g_{ds4} + g_{ds1}} \left[ \frac{1 - s C_{gds1}}{g_{m1}} \right] \frac{g_{m1}}{1 + \left( \frac{C_{Leq} + C_{gds1}}{g_{ds4} + g_{ds1}} \right) s} \]

RHP Zero:\( f_z = \frac{g_{m1}}{2 \pi C_{gds1}} \), \( f_z > f_p \)

LHP Pole:\( f_p = \frac{g_{ds4} + g_{ds1}}{2 \pi (C_{db4} + C_{db1} + C_L + C_{gds1})} \)

\[f_u \quad \Box\quad A_d f_p = \frac{g_{m1}}{2 \pi (C_{db4} + C_{db1} + C_L + C_{gds1})} \]

2. Common-mode half circuit:

\[(g_{ds4} + sC_M) V_{oc} + g_{ds1} (V_{oc} - V_S) + g_{m1} (V_{ic} - V_S) + C_{gds1} s (V_{oc} - V_{ic}) = 0\]
\[ g_{ds1}(V_i - V_{oc}) + V_i \left( \frac{1}{2r_{ds5}} + \frac{C_{gd5} + C_{db5} + C_{sbl}}{2} \right) - g_{ml}(V_i - V_s) - C_{gs1}s(V_i - V_s) = 0 \]

\[ V_s \left[ \frac{1}{2r_{ds5}} + \frac{1}{2} \left( \frac{C_{gd5} + C_{db5} + C_{sbl}}{2} \right) s + C_{gs1}s \right] = -\left[ g_{ds4} + sC_M + sC_{gd1} \right] V_{oc} + (C_{gs1} + sC_{gd1}) V_i \]

\[ V_s = -\left[ \frac{g_{ds4} + sC_M + sC_{gd1}}{2} \right] V_{oc} - \left( \frac{C_{gs1} + sC_{gd1}}{2} \right) V_i \]

\[ \Rightarrow A_c(s) = \frac{V_{oc}}{V_i} = \frac{-C_{gd1} \left( \frac{C_{gd5} + C_{db5} + C_{sbl}}{2} + C_{gs1} \right) s^2 + \left( \frac{C_{gd5} + C_{db5} + C_{sbl}}{2} + C_{gs1} \right) g_{ml}} {C_{gd5} + C_{db5} + C_{sbl} + C_{gs1} \left( C_M + C_{gd1} \right) s^2 + \left( C_{gd5} + C_{db5} + C_{sbl} + C_{gs1} \right) g_{ml}} \]

\[ \Rightarrow 1 \text{ RHP zero, } 1 \text{ LHP zero, } 2 \text{ LHP poles} \]

Solve the pole-zero position: 

\[ A_c(s) = \frac{V_{oc}}{V_i} \]

\[ dB, \quad CMRR \]

\[ f_{ZL}, \quad f_{ZL} \]

\[ f_{p1}, \quad f_{p2} \]

\[ f_{ZL} \quad \Rightarrow \quad f_{p1} \quad f_{p2} \]

\[ CM \quad (C_{gd5} + C_{db5} + C_{sbl}) / 2 \]

Load pole 

Tail pole 

Degradation region
6-1.6 CMOS differential-input-to-single-ended output converter

\[ V_i = V_{id} + V_{ic} \quad V_o = V_{od} + V_{oc} \]

* The hail-circuit method cannot be used in the high frequency analysis.

* Two unequal signal paths to the output
  \( \Rightarrow \) Load path and tail path
  \( \Rightarrow \) Both \( C_s \) and \( C_E \) appears in the \( A_d(s) \) expression.

* There are two dominate poleo in \( A_d \).

Output pole
\[ W_{p1} \approx \frac{g_{ds1} + g_{ds4}}{C_{Leq}} \]

Mirror pole
\[ W_{p2} \approx \frac{g_{m34}}{C_E} \]

Tail path:
\[ A_1(s) = \frac{A_0}{1 + \frac{s}{W_{pl}}} \]

Load path:
\[ A_2(s) = \frac{A_0}{(1 + \frac{s}{W_{p1}})(1 + \frac{s}{W_{p2}})} \]

\[ A_d(s) = A_1(s)A_2(s) = \frac{A_0(2 + \frac{s}{W_{p2}})}{(1 + \frac{s}{W_{p1}})(1 + \frac{s}{W_{p2}})} \]

LHP zero:
\[ W_{z1} \approx \frac{2g_{m34}}{C_E} = 2W_{p2} \]

* Approximate analysis:

The dominant pole of \( A_d(s) \) is
\[ S_{pl} = g_{ds1} + g_{ds4} \quad (output \ pole) \]

\[ A_d(s) \approx \frac{g_{m1}}{SC_{Leq} + (g_{ds1} + g_{ds4})} \]
The $A_c(s)$ can be written as:

$$A_c(s) \equiv -\frac{g_{ds1}}{2g_{m1}} \frac{(1)}{s} + sC_s + \frac{g_{ds1} + g_{ds4}}{C_{Leq}}$$

The dominant pole of $A_c(s)$ is:

$$s_{p1} = \frac{g_{ds1} + g_{ds4}}{C_{Leq}}$$

But the left-half-plane zero is:

$$s_{zL} = -\frac{1}{R_0} \left( \frac{1}{s} \right)$$

The CMRR ($\equiv \frac{A_d}{A_c}$) is degraded by 20dB/decade at high frequency.

§6-2 Frequency Compensations

Without $C_C$:

$$S_{p1} = -\frac{I}{C_d} (g_{dit} + g_{dzi}) \ , \quad S_{p2} = -\frac{I}{C_L} (g_{dsgl} + g_{dsg2})$$
\[ H(s) = \frac{v_2}{v_o - v_2} + g_m(g_{mg1} + g_{mg2})R_dR_c\left(1 - \frac{sC_c}{g_{mg1} + g_{mg2}}\right) \]
\[ = \frac{1 + s\left[(C_L + C_c)R_o + (C_c + C_d)R_d + C_c(g_{mg1} + g_{mg2})R_oR_d\right]}{1 + s\left[(C_cL + C_cC_d + C_dC_L)R_oR_ds^2\right]} \]

where \( R_o \equiv -\frac{1}{g_{dgi} + g_{dgi2}} \quad R_d \equiv -\frac{1}{g_{dis} + g_{disl}} \)

\[ \Rightarrow S_{p1} \approx -\frac{1}{(g_{mg1} + g_{mg2})R_oR_dC_c} \quad S_{p2} \approx -\frac{C_c(g_{mg1} + g_{mg2})}{C_oC_cL + C_dC_cL + C_dC_c} \]

\[ S_c \approx \frac{g_{mg1} + g_{mg2}}{C_c} \Rightarrow \text{RHP Zero} \]

* Feedforward effect on \( C_c \)

How to solve this problem?

If \( I_{cc} = (g_{mg1} + g_{mg2})V_d \),

\[ I_o = 0 \quad \text{and} \quad V_2 = 0 \]

\( \Rightarrow \) A zero is formed.
§6-2.1 Using a unity-gain buffer in the feedback path

* Isolate node 1 from node 2 to prevent feedforward.
* Keep the Miller effect unchanged.
* Source follower can act as a unity gain buffer.

\[
\begin{align*}
g_{m1} V_d + \frac{V_i}{R_d} + C_d s V_i + (V_i - V_2) C_c s &= 0 \quad \text{-------- (1)} \\
(g_{mg1} + g_{mg2}) V_i + \frac{1}{R_o} V_2 + C_L s V_2 &= 0 \quad \text{-------- (2)} \\
H(s) &= \frac{V_2}{V_d} \\
&= \frac{g_{m1} (g_{mg1} + g_{mg2})}{1 + s [R_o C_c + R_d (C_d + C_c) + C_c (g_{mg1} + g_{mg2}) R_o R_d] + (C_c C_L + C_d C_L) R_o R_d s} \\
S_{p1} &\approx -\frac{1}{(g_{mg1} + g_{mg2}) R_o R_d C_c} \quad \text{(unchanged)} \\
S_{p2} &\approx -\frac{C_c (g_{mg1} + g_{mg2})}{C_c C_L + C_d C_L} \quad \text{RHP Zero has been eliminated.}
\end{align*}
\]
Actual Circuits:

\[
\begin{align*}
V_{DD} & \quad M_1 \quad V_{BIAS} \\
C_C & \quad V_1 \\
-V_{SS} & \quad M_2 \\
& \quad V_2
\end{align*}
\]

\[
\begin{align*}
V_{BIAS} \text{ or} \\
\text{connected to the} \\
\text{output}
\end{align*}
\]

\[
\begin{align*}
C_{gs1} & \text{may introduce a RHP zero. But usually this RHP zero is large.} \\
C_{gs1} & \text{is very small.}
\end{align*}
\]

\[
R_{out} \approx \left( \frac{1}{g_{m1}} \right) \left( \frac{1}{g_{m2}} \right)
\]

\[
g_{m1} V_d + \frac{V}{R_d} + C_d s V_1 + (V_1 - \alpha V_2) \left( \frac{1}{C_s} + \frac{1}{R_{out}} + C_{out}s \right)^{-1} = 0
\]

If \( \frac{1}{R_{out}} \geq C_{out}s \)

\[
\Rightarrow \left( \frac{1}{C_s} + \frac{1}{R_{out} + C_{out}s} \right)^{-1} \approx \frac{C_s}{C_s R_{out}s + 1}
\]
The numerator of \( H(s) = \frac{V_2(s)}{V_d(s)} \) is \( g_{m_i}(g_{mg1} + g_{mg2})(C_{out}s + 1) \)

\[ \Rightarrow \text{LHP Zero} : \quad -\frac{1}{C_c R_{out}} \]

If \( R_{out} \) is large, LHP Zero may form a pole-zero doublet with \( S_{p1} \) or \( S_{p2} \).

\[ \Rightarrow \text{very slow slew rate} !! \]

If \( R_{out} \) is small, too large \( g_{m1} \) or \( g_{m2} \) is required.

\[ \Rightarrow \text{(large area, large power)} \]

\[ \Rightarrow \text{large } C_{out}. \quad \text{Freq. Resp.} \quad \square \]

* Somehow difficult to design.

* Also the power dissipation of the buffer is large. (additional power dissipation)

§6-2.2 Adding \( R_c \) in series with \( C_c \).

\[ H(s) = \frac{V_2}{V_d} \text{ can be solved.} \]

Low frequency gain : \( A_{dm} = g_{m_i}(g_{mg1} + g_{mg2})R_o R_d \)

LHP Poles : \( S_{p1} \equiv -\frac{1}{(g_{mg1} + g_{mg2})R_o R_d C_c} \) \quad (unchanged)

\[ S_{p2} \equiv -\frac{(g_{mg1} + g_{mg2})C_c}{C_d C_L + C_c C_L + C_c C_c} \] \quad (unchanged)

\[ S_{p3} \equiv -\frac{C_c C_c + C_d C_c + C_c C_L}{R_c C_d C_c C_c} \]

\[ \left( \begin{array}{c}
\text{LHP} \\
\text{RHP}
\end{array} \right) \text{Zero : } S_Z = -\frac{g_{mg1} + g_{mg2}}{C_c [R_c (g_{mg1} + g_{mg2}) - 1]} \]
1. If \( R_c = \frac{l}{g_{mg1} + g_{mg2}} \) or \( R_c = \frac{l}{g_{m2}} \): second-stage transconductance

\( S_Z \rightarrow \pm \infty \) No effect on the frequency response of the OP.

\( S_{p1} \) dominant pole \( \Rightarrow A_d(s) = \frac{A_{dm}S_{p1}}{s + S_{p1}} \)

For \( \omega >> S_{p1} \) \( A_d(j\omega) = \frac{A_{dm}S_{p1}}{j\omega} \), \( |A_d(j\omega)| = \frac{A_{dm}S_{p1}}{\omega} \)

At \( \omega_u \), \( |A_d(j\omega_u)| = 1 \) \( \Rightarrow \omega_u = A_{dm}S_{p1} = \frac{g_{mi}}{C_c} \)

Large \( C_L \Rightarrow S_{p2} \approx -\frac{g_{mg1} + g_{mg2}}{C_L} \)

For phase margin \( 45^\circ \sim 60^\circ \) \( \Rightarrow \frac{S_{p2}}{\omega_u} \equiv 2 \sim 4, \frac{C_c}{C_L} \frac{g_{mg1} + g_{mg2}}{g_{mi}} = 2 \sim 4 \)

If \( \frac{g_{mi}}{g_{mg1} + g_{mg2}} \approx 2 \sim 4 \), \( C_L \equiv C_c \) stable

1) NMOS Realization:

\[ \begin{align*}
V_{DD} & \quad C_c \quad M_c \\
\text{phase} & \quad 0^\circ \quad -45^\circ \quad -90^\circ \quad -135^\circ \quad -180^\circ \\
V_1 & \quad V_2 \quad -V_{SS}
\end{align*} \]
\[ I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[ 2(V_{DD} - V_2 - V_{TH}) V_{DS} - V_{DS}^2 \right], \]

\[ R_c = \left( \frac{\partial I_{DS}}{\partial V_{DS}} \right)_{\text{Vos=0}} = \frac{1}{\mu_n C_{ox}} \frac{W}{2 L} \left[ 2(V_{DD} - V_2 - V_{TH}) \right] \]

\( V_2 \uparrow V_{TH} \uparrow \) body effect

Design \( R_c \): 
1. Design \( R_c \), s.t. \( (R_c)_{V_2=0V} = \frac{I}{g_{m2} + g_{m2}^2} \)

2. At \( R_c = R_{cmax} \) or \( R_{cmin} \),
   \( S_z \) must be large enough! Otherwise, frequency performance will be degraded.

1) CMOS Realizations:

Consider the case in c.:

\[ I_{DSn} = \frac{\mu_n C_{ox}}{2} \frac{W_n}{L_n} \left[ 2(V_{DD} - V_2 - V_{THn}) V_{DS} - V_{DS}^2 \right] \]

\[ R_{cn} = \frac{1}{\mu_n C_{ox}} \frac{W_n}{2 L_n} \left[ 2(V_{DD} - V_2 - V_{THn}) \right] \]
\[ I_{DSP} = \frac{\mu_p C_{ox} W_p}{2 L_p} \left[ 2(V_2 + V_{SS} - V_{Thp}) V_{DS} - V_{DS}^2 \right] \]

\[ R_{cp} = \frac{L_p}{\frac{\mu_p C_{ox} W_p}{2} \left[ 2(V_2 + V_{SS} - V_{Thp}) \right]} \]

\[ R_{c}^{-1} = (R_n \parallel R_{cp})^{-1} = R_n^{-1} + R_{cp}^{-1} \]

\[ R_{c}^{-1} = \frac{\mu_n C_{ox} W_n}{2 L_n} \left[ 2(V_{DD} - V_2 - V_{Thn}) \right] + \frac{\mu_p C_{ox} W_p}{2 L_p} \left[ 2(V_2 + V_{SS} - V_{Thp}) \right] \]

If \( \frac{\mu_n C_{ox} W_n}{2 L_n} = \frac{\mu_p C_{ox} W_p}{2 L_p} = \beta \)

\[ R_{c}^{-1} = \beta \left[ 2V_{DD} - 2V_{Thn} + 2V_{SS} - 2V_{Thp} \right] \text{ nearly indep. Of } V_2 \]

\[ R_{c}^{-1}\bigg|_{V_2=0V} = g_{mg1} + g_{mg2} \]

2. If \( R_c = \frac{I + (C_d + C_L) / C_p}{g_{mg1} + g_{mg2}} \)

\( S_z = S_{p2} \) and pole-zero cancellation occurs.

\( \Rightarrow S_{p3} >> S_{p1} \Rightarrow A_{dm} S_{p1} < S_{p3} \Rightarrow \text{stable} \)

However, if the cancellation is not complete

\( \Rightarrow \text{pole-zero doublet occurs!} \Rightarrow \text{slow slew rate.} \)
§6-2.2 Feedforward compensation

\(A_{v3}\) is the gain of the source follower

\[
\begin{align*}
A_{v3} &= \frac{A_v(0)(1 + \frac{s}{z_j})}{(1 + \frac{s}{P_3})} & 1 \text{ LHP zero} \\
&= \frac{A_v(0)(1 - \frac{s}{z_1})(1 + \frac{s}{z_2})}{(1 + \frac{s}{P_1})(1 + \frac{s}{P_2})} & 2 \text{ LHP poles} \\
&\quad 1 \text{ RHP zero (C_C)} \\
&\quad 1 \text{ LHP zero}
\end{align*}
\]

\(z_3\) & \(z_2\) are generated from the \(C_{gs}\) of the source follower.

\[
\frac{V_{out}}{V_{in}} = A_{vTOR}(s) = A_{v2}(s) + A_{v3}(s) \\
= [A_{v2}(0) + A_{v3}(0)] \frac{(1 + \frac{s}{z_1})(1 + \frac{s}{z_2})(1 + \frac{s}{z_3})}{(1 + \frac{s}{p_1})(1 + \frac{s}{P_1})(1 + \frac{s}{P_2})}
\]

\(p_1\) : dominant pole

\(z_1', z_2', z_3'\) : LHP Zeros

Design consideration: Any zeros below the unity-gain frequency must be placed as close as possible to their matching poles.

This prevents the formation of any doublet!

\(z_1' = p_2\) by adding CB1 and CB2(3.8pF) to control \(C_{gs9} + C_{gs11}\)
6-3 Settling Behavior

Slewing Period ($T_s$): $V_o$ from 0V to $V-I_i/g_{mi}$ under voltage follower connection and worse case loading (nonlinear operation)

Settling Period ($T_{SET}-T_s$):

$V_o$ from $(V-I_i/g_{mi})$ to $\pm 0.1\%V$ or $\pm 0.01\%V$ (quasi-linear operation)

Settling Time ($T_{SET}$): $T_s + (T_{SET}-T_s) = $ slewing period + settling period.

6-3.1 Single-pole case
Slew rate:

\[ SR = \frac{dV_o}{dt}\bigg|_{\text{max}} = \frac{I_o}{C_c} \]

\[ \omega_u = \frac{g_{m_1}}{C_c} \leftarrow \text{single-pole case} \]

\[ SR = \frac{I_o \omega_u}{g_{m_1}} = \omega_u \sqrt{\frac{I_o}{2uC_{ox}(\frac{W}{L})}} \]

6-3.1 Two-pole case

Ref: IEEE JSSC vol.SC-17, no.1 pp.74-80, Feb. 1982

\[ T_s = -\frac{1}{\omega_1} \ln \left[ 1 - \frac{g_{m_1}}{I_o a_o} (V - \frac{I_o}{g_{m_1}}) \right] \]

approximation: \( e^{-\omega_1 T_s} \equiv 1 - \omega_1 T_s = \Rightarrow \text{eq.(19) conventional expression} \)

After \( T_s \):

\[ V_o = V - \frac{I_o}{g_{m_1}} \]

Input voltage = \( V - (V - \frac{I_o}{g_{m_1}}) = \frac{I_o}{g_{m_1}} \)

\[ \Rightarrow \text{enter the linear (or quasi-linear) region} \]

Feedback Function for unity-gain voltage-follower connection

\[ A(s) = \frac{a(s)}{1 + a(s)} \quad \text{eq.(20)-(23)} \]

two poles: \( S = -\xi \omega_n \pm \sqrt{\xi^2 - 1} \omega_n \quad \text{eq.(24)} \)

\[ \xi = \frac{\omega_1 + \omega_2}{2\omega_n} \quad \text{(double negative real poles)} \]

\[ \text{damping ratio} \]

\[ \text{Critically damped: } \xi = 1 \]

\[ \text{Underdamped: } \xi < 1 \]

\[ \text{Overdamped: } \xi > 1 \]

\[ (\text{complex conjugate poles}) \quad (\text{real and negative pole}) \]

\[ \xi = \frac{\omega_1 + \omega_2}{2\omega_n} \approx \frac{\sqrt{\omega_2}}{2\sqrt{\omega_n a_1}}, \frac{\sqrt{\omega_2}}{2\sqrt{\omega_n a_2}} = \frac{\sqrt{\frac{g_{m_1}}{c_2}}}{2\sqrt{\frac{g_{m_1}}{c_1}}} \quad (C_C, C_2 >> C_1) \]
\[ \xi \ll 1 \implies C_c \ll 4 \left( \frac{g_{m1}}{g_{m2}} \right) C_2 \quad (C_C, C_2 >> C_1) \]

\[ \implies \omega_2 \ll 4 \omega_u \iff \frac{\omega_2}{\omega_u} = 2 \sim 4 \quad \omega_2 < 4 \omega_u \quad \text{underdamped} \]

\[ \omega_2 > 4 \omega_u \quad \text{overdamped} \]

(1) Underdamped: \( T_s \) eq. (14) or (19) \quad \text{max. overshoot: eq.(36)}

\[ T_P \text{ eq. (35), (33)} \quad \text{settling time: eq.(40),(39)} \]

(2) Critically Damped \( V_o(t) \): eq.(41)

\[ T_{SET} : \text{eq.(43)} \]

(3) Overdamped \( T_{SET} : \text{eq.(47)} \)

Simulation & Calculation : Fig.7, Fig.8

Further references:


(2) *IEEE JSSC*, vol. SC-21, pp.478-483, June. 1986
§ 6-4 Slew rate of CMOS OP AMPs

§ 6-4.1 Two-stage OP AMPs

Two poles: \( S_{p1}, S_{p2}, |S_{p1}| << |S_{p2}| \)

If \( |S_{p1}| << \omega_u << |S_{p2}|, V_{out}(s) = g_{mi} V_{in}(s) / s C_c \)

\[
\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{g_m}{j\omega C_c}
\]

At \( \omega = \omega_u , \frac{V_{out}}{V_{in}} = 1 \)

\[ \Rightarrow \omega_u = \frac{g_{mi}}{C_c} \quad \text{or} \quad C_c = \frac{g_{mi}}{\omega_u} \]

The slew rate \( SR = \frac{dV_{out}}{dt} \bigg|_{max} = \frac{I_o / C_c}{I_c} = \frac{I_c \omega_u}{g_{mi}} = \omega_u \sqrt{\frac{I_o}{2u C_o (W / L)}} \)

\( \omega_u \uparrow, I_o \uparrow \left( \frac{W}{L} \right) \downarrow \Rightarrow SR \uparrow \)

* \( I_o / C_L \geq I_o / C_c \) or \( C_L \frac{dV_{out}}{dt} \leq C_c \frac{dV_{out}}{dt} \) (\( = I_o \))

Slew rate enhancement and degradation
(1) Positive step

\[ i_o(t) = C_\infty \frac{dv_o(t)}{dt} \equiv C_\infty \frac{dv_o(t)}{dt} \]

\[ v_{out}(t) = \frac{I}{C_C} \int_0^t (I + i_o) dt = \frac{I_o}{C_C} t + \frac{C_\infty}{C_C} \frac{dv_{in}}{dt} dt \]

\[ = \frac{I}{C_C} t + \frac{C_\infty}{C_C} v_{in}(t) \]

(2) Negative step
\[ v_{out} \approx v_o \]
\[ \frac{d}{dt}v_{out} = -\frac{I_o - i_o}{C_C} = \frac{dv_o}{dt} = -\frac{i_o}{C_o} \Rightarrow i_o = \frac{I_oC_o}{C_C + C_o} \]

\[ \frac{dv_{out}}{dt} = -\frac{I_o}{C_C + C_o} \text{ slew degradation} \]

§ 6-4.2 Single-stage OP AMPs

\[ SR = \frac{I_o}{C_L} \]

Different phase margins

⇒ different settling behavior.

\( I_o \): First-stage bias current

SR of the folded cascode OP AMPs

\[ SR = \frac{I_o}{C_L} \]

* If \( I_p = I_o \), we can keep \( M_5, M_1 \) and \( I_o \) current source in saturation.
The change of $V_x$ is not significant because the gain of the common-source amplifier $M_1$ is nearly equal to $-1$. When $M_2$ is turned on, the recovery time of $V_x$ is very short.

* If $I_p < I_o$, the current source $I_o$ is forced to linear region and $V_x \downarrow$, $V_x \downarrow$. The decrease of $V_x$ is large. Thus the recovery time of $V_x$ when $M_2$ is turned on is very long, $\Rightarrow$ The settling is slow down.

How to solve this problem?

(1) Keep $I_p = I_o$ as the optimal design.

(2) Add clamping devices between $V_{DD}$ and $V_s(V_Y)$

In normal operation, $M_{11}$ and $M_{12}$ are turned off by setting $V_{DD} \cdot V_x < V_{TH11}, V_{TH12}$.

§ 6-5 Power supply rejection ratio (PSRR)

§ 6-5.1 Low frequency analysis for integrators
\[
\frac{\partial V_{out}}{\partial V_{SS}} = \frac{C_{gs}}{C_1} \left[ \frac{\partial I_o}{\partial V_{SS}} \frac{1}{2g_{m1}} + \frac{\partial V_{GS1}}{\partial V_{SS}} \right] + \frac{C_{gd}}{C_1} \frac{1}{2g_{m3}} \frac{\partial I_o}{\partial V_{SS}}
\]

\[
\frac{\partial V_{out}}{\partial V_{DD}} = -\frac{C_{gs}}{C_1} \left[ 1 - \frac{\partial I_o}{\partial V_{DD}} \frac{1}{2g_{m3}} \right] + \frac{C_{gd}}{C_1} \frac{1}{2g_{m1}} \frac{\partial I_o}{\partial V_{DD}}
\]


* \(C_{gs}/C_1\) and \(C_{gd}/C_1\) have a strong effect on PSRR\(^+\) and PSRR\(^-\).

* Small \(C_1\) ⇒ chip area ↓ but PSRR ↓.

§ 6-5.2 High frequency analysis for OP AMP’s

\[ PSRR^* = \left[ \frac{\partial V_o}{\partial V_i} \right] = \left[ \frac{\partial V_o}{\partial V_{DD}} \right]_{V_i=0} = \left[ \frac{\partial V_{io}}{\partial V_{DD}} \right]_{V_i=0}^{-1} \]

How to calculate \( \frac{\partial V_{io}}{\partial V_{DD}} \)?

\[ PSRR^*(s) = \frac{s + G_{o1}G_{o2} / (g_{m2}C_c)}{s + g_{m1} / C_c} \]

where \( G_{o1} = g_{o4} \) (\( g_{o2} \) is connected to the drain of \( M_5 \) which is open-circuited, i.e. \( r_{ds5} \rightarrow \infty \))

\[ G_{o2} = g_{o6} \] (\( r_{ds7} \rightarrow \infty \))

\[ G_{o1}G_{o2}/(g_{m2}C_c) < g_{m1}/C_c \]

\( \Rightarrow \) Low-frequency LHP zero degrades the \( PSRR \).
To improve PSRR, $C_c$ must be decoupled from the gate of $M_6$ to eliminate the LHP zero.
Chapter 7 Design Procedure of CMOS OP AMPs and Practical Design Considerations on Noise and Offset

§ 7-1 Typical design procedure of two-stage CMOS OP AMPs

Synthesis or Design: Determine the circuit configuration and its MOS device dimensions from the specifications.

Flow Diagram:

1. Specifications
2. Choose suitable OP AMP configurations
3. Design Procedures set-up to determine W/L
4. Full SPICE simulation
5. Layout and verification
6. Resimulation
Specifications

- Low frequency gain \( \geq 70\text{dB} \)
- Phase margin \( > 60^\circ \)
- Unity-gain frequency \( \geq 2\text{MHz} \)
- \( C_L = 10\text{pF} \)
- Slew rate \( \geq 4\text{V/\mu s} \)
- \( V_{DD}=V_{SS} = 5\text{V} \)
- CMRR \( \geq 80\text{dB} \)

Device parameters

\[
\begin{align*}
\frac{\mu C_{os}}{2} & : 30\mu\text{A/V}^2 \\
(\text{NMOS}) & : 12\mu\text{A/V}^2 \\
V_{TO} & : 1.2\text{V} \\
& : -1\text{V}
\end{align*}
\]

Procedures:

1. Choose a suitable \( C_c \)
   - Example: choose \( C_c=C_L=10\text{pF} \)
2. According to the phase margin in the specifications, determine the second pole position.
Example: choose $f_T = 2$MHz

$$|S_{p2}| = + \frac{g_{m6}}{C_L} = 3 \omega_u \equiv \frac{3 g_{m6}}{C_C}$$

$$|S_{p2}| = 3 \omega_u \Rightarrow \text{Phase margin} > 60^\circ$$

3. Determine the transconductances of the first stage and the second stage.

Example: $g_{m6} = 3 g_{m1} = 3 \omega_u C_L = 3 \times 2\pi \times 2 \times 10^6 \times 10^{-11}$

$$\Rightarrow g_{m6} = 377 \mu \text{ mho}$$

$$g_{m1} = 125.7 \mu \text{ mho}$$

4. From the slew rate specification, determine the bias currents in the first and the second stages.

Example: $S = \frac{I_o}{C_C} \geq 4 \text{V/\mu s}$

Choose $S = 4 \text{V/\mu s}, \Rightarrow I_o = 40 \mu A$

The negative-going slew rate is also limited by the $Q_7$ current source. To reduce or eliminate its effect, $S_{r_o}$ is set to 4S.

$$S_{r_o} = 2.5S = 10 \text{V/\mu s} = \frac{I_o}{C_L}$$

$$\Rightarrow I_7 = C_4 S_{r_o} = 100 \mu A$$

5. Use the design rule for reducing the systematic offset voltage to design the transconductance of the load MOSFET’s.

Example:

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_3}{(W/L)_6} = \frac{I_o/2}{I_7} = \frac{1}{5}$$

$$g_{m1} = g_{m3} = g_{m4} = \sqrt{\frac{(W/L)_3 \cdot I_o/2}{(W/L)_6 \cdot I_7}} g_{m6}$$

$$= \frac{I_o/2}{I_7} g_{m6} = \frac{1}{5} g_{m6} \equiv 75.4 \mu \text{ mho}$$
6. Calculate $A_{dm}$ and CMRR to verify the design.

Example: $A_{dm} = \frac{g_{mi}g_{m6}}{(g_{di} + g_{m6})(g_{d6} + g_{d7})} \approx \frac{g_{mi}g_{m6}}{(\lambda I_o)(2\lambda I_\gamma)}$ 

$\approx 6582 > 76\,\text{dB} \quad (\lambda = 0.03\,\text{V}^{-1} \text{ for } L \approx 10\,\mu\text{m})$

$CMRR = 2\frac{g_{mi}g_{m6}}{g_{d3}g_{di}} \approx \frac{2g_{mi}g_{m6}}{(\lambda I_o)(\lambda I_o/2)} \approx 26327 \approx 88\,\text{dB}$

$g_{mi} = C_vW_u, \quad I_o = C_vS, \quad g_{m6} = 3W_uC_L, \quad I_7 = S_{ro}C_L$

$g_{mi} = I_o g_{m6}/2I_7 = 3C_vSW_u/2S_{ro}$

$\Rightarrow A_{dm} \approx \frac{3\omega^2_u}{2\lambda^2 S_{ro}S} ; \quad CMRR \approx \frac{6\omega^2_u}{\lambda^2 S_{ro}S} \approx 4A_{dm}$

If $A_{dm}$ and $CMRR$ could not satisfy the specifications, $\omega_u$, $S$, and $g_{mi}$ or $g_{m6}$ can be readjusted.

7. Determine the nulling resistor $R_c$ provided by $M_8$.

Example: If $S_2 \rightarrow S_{p2}$

$$R_c = \frac{1 + (C_d + C_L)/C_v}{g_{m6}} \approx \frac{2}{g_{m6}} \approx 5.3\,\text{k}\Omega$$

If $S_2 \rightarrow \infty$

$$R_c = \frac{1}{g_{m6}} = 2.65\,\text{k}\Omega$$

$$R_c = \frac{1}{\mu_p C_{ox} \frac{W_8}{L_8} \left[2(V_{SS} + V_B - |V_{TH8}|)\right]}$$

8. Dimension $M_5$ and $M_7$.

$W/L$ can’t be too small $\Rightarrow$ too large $V_{GS}$.

Can’t be too large $\Rightarrow$ $C_w$ too large $\Rightarrow$ CMRR $\downarrow$

$C_L \uparrow$ $\Rightarrow$ phase margin $\downarrow$
Example: \( \left( \frac{W}{L} \right)_5 = \frac{I_o}{\frac{\mu_n C_{ox}}{2} (V_{GS5} - V_{TH5})^2} \approx 5.33 \) (\( \frac{\mu_n C_{ox}}{2} \approx 30 \mu A/\sqrt{V} \))

\( V_{GS5} - V_{TH5} \approx 0.5V \)

\( \left( \frac{W}{L} \right)_7 = \frac{I_7}{\frac{\mu_n C_{ox}}{2} (V_{GS7} - V_{TH7})^2} \approx 13.33 \)

Choose \( L_5 = L_7 = 10 \mu m \Rightarrow W_5 = 54 \mu m \), \( W_7 = 133 \mu m \)

9. Dimension \( M_1 - M_4 \) and \( M_6 \)

Example: \( g_m \approx 2 \sqrt{\frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_D} \)

\( \left( \frac{W}{L} \right)_1 = \left( \frac{W}{L} \right)_2 \approx \frac{8m_i^2}{4 \frac{\mu_n C_{ox} I_o}{2} / 2} \approx 6.58 \)

\( (W/L)_3 = (W/L)_4 \approx \frac{g_{ml}^2}{4 \frac{\mu_p C_{ox} I_o}{2} / 2} \approx 5.92 \)

\( (W/L)_6 = 5(W/L)_3 \approx 29.6 \)

Choose \( L = 10 \mu m \)

\( \Rightarrow W_1 = W_2 = 66 \mu m \), \( W_3 = W_4 = 60 \mu m \), \( W_6 = 300 \mu m \)

10. Estimate the dc bias voltage.

Example: \( |V_{GS3}| = |V_{THP3}| + \frac{I_o / 2}{\sqrt{\frac{\mu_p C_{ox}}{2} (W/L)_3}} = 1 + \sqrt{\frac{20}{12 \times 6}} \approx 1.527 \)

\( \Rightarrow V_A = V_B = V_{DD} - |V_{GS3}| = 3.473V \)

\( \frac{I_o}{2} = \frac{\mu_n C_{ox}}{2} (W/L)_1 (-V_C - V_{THn})^2 \)

\( \Rightarrow V_C = -1.518V \)

11. Dimension \( M_8 \)
Example: \[ 2 \frac{\mu_p C_{ox}}{2} (W / L)_8 (5 + 3.473 - 1) = \frac{1}{R_C} \]

\[ \Rightarrow (W / L)_8 \approx 1.052 \]

choose \( W_8 = L_8 = 10 \mu m \).

12. Determine \( V_{BLAS} \) and dimension \( M_g \) and \( M_{i0} \)

Example: \( V_{GS} = V_{THn} + 0.5V = 1.7V \)

\[ V_{BLAS} = -V_{SS} + V_{GSS} = -3.3V \]

Choose \( I_b = 20 \mu A \)

\[ \Rightarrow V_{GS9} = 0 - V_{BLAS} = 3.3V \Rightarrow V_{BLAS} = -3.3V \]

\( V_{GS10} = V_{BLAS} + V_{SS} = -1.7V \)

\[ (W / L)_9 = \frac{I_b}{\frac{\mu_n C_{ox}}{2} (V_{GS9} - V_{THn})^2} \approx 0.1512 \]

\[ (W / L)_{10} = \frac{I_b}{\frac{\mu_n C_{ox}}{2} (V_{GS10} - V_{THn})^2} \approx 0.2667 \]

Choose \( W_9 = 10 \mu m \), \( L_9 = 66 \mu m \) and

\( W_{10} = 27 \mu m \), \( L_{10} = 10 \mu m \).

13. Use SPICE to simulate the overall OP AMP and make the necessary adjustment.

§7-2 Practical Design Consideration on Noise

§7-2.1 Noise of MOS devices

1) shot noise

* Due to the fluctuation in the number of carriers crossing a given surface in the conductor in any time interval.

* If the carrier density is low and the external electric field is high so that the interaction among the carriers are negligible, we have

\[ \overline{i_{ns}^2} = 2qI(BW) \]

where \( i_{ns} \) is the random variation of the current.

I is the average current.

BW is the bandwidth in which the noise is measured.

* When an MOSFET is operated in the saturation region, inversion carrier density is high. \( \Rightarrow \overline{i_{ns}^2} \) is much smaller than that predicted by the formula.

Shot noise is not important.

* In the subthreshold region, shot noise is higher.

2) Thermal noise

* Generated by the random thermal motion of the carriers in a resistor.

* The mean square of the noise voltage \( v_{nT} \) and the noise current \( i_{nT} \) are

\[ \overline{v_{nT}^2} = 4KTR(BW) \]

\[ \overline{i_{nT}^2} = 4KTG(BW) \]

* In MOSFETs, R is the incremental channel resistance.

If the MOSFET is in the saturation region, \( R = \frac{3}{2g_m} = \frac{1}{\frac{2}{3}g_m} \)

\[ \overline{v_{nT}^2} = \left( \frac{i_{nT}}{g_m} \right)^2 = \frac{8}{3} \frac{KT}{g_m} BW \]

* The spectral density \( \frac{\overline{v_{nT}^2}}{BW} \) is independent of frequency \( \Rightarrow \) White noise.

* Circuit models:

\[ \overline{v_{nT}^2} : \text{gate-referred noise voltage source.} \]
\[
* \frac{\sqrt{\frac{V_{nt}^2}{BW}}}{\sqrt{H_z}} = \frac{nV}{\sqrt{H_z}}
\]

* When the MOSFET is turned off (R=\(\infty\), G=0), \(\overline{i_{nf}}\) is very small.

\[\Rightarrow \] Noiseless open circuit.

3) Flicker \((\frac{1}{f})\) noise

* Generated by the trapping and releasing electrons from the channel caused by the interfacial states.

* Slow process \(\Rightarrow\) important at low frequencies

\[\Rightarrow \frac{1}{f} \text{ noise. Below } \sim KH_z\]

\[
* \overline{v_{nf}} = \frac{K BW}{C_{oxWL}} \frac{i_{nf}^2}{f} \quad i_{nf}^2 = g_m^2 v_{nf}^2
\]

*(WL) \(\uparrow\), \(C_{ox} \uparrow\), Temperature \(\downarrow\), density of surface state \(\downarrow\) \(\Rightarrow\) \(v_{nf}^2\) \(\downarrow\)

4) Combined noise

\[
i_n = \sqrt{i_{nf}^2 + i_{nf}^2} = \sqrt{(4KTG + Kg_m^2/(C_{oxWL})\)BW}
\]

\[\Rightarrow \text{ independent noise sources.}\]

\[
v_n = \frac{i_n}{g_m}
\]

§7-2.2 Noise Performance of NMOS Amplifiers

1) Enhancement-load amplifier

\[
A_{v1} = -\alpha_2 \sqrt{\frac{W_1L_2}{W_2L_1}} \quad \text{for } e_{n1}
\]

\[
A_{v2} = \alpha_2 \quad \text{for } e_{n2}
\]

The equivalent input noise voltage

\[
e_n (IN) = \frac{1}{A_{v1}} \overline{(A_{v1}e_{n1})^2 + (A_{v2}e_{n2})^2}
\]

\[= e_{n1} \sqrt{1 + \left(\frac{A_{v2}e_{n2}^2}{A_{v1}e_{n1}^2}\right)}
\]

\[= \frac{a_n}{\sqrt{W_1L_1(1 + \frac{L_1}{L_2})^2}}
\]

\[e_n : \text{1/f noise}\]

\[
e_n = \frac{a_n}{\sqrt{W_1L}}
\]
§7-2.3 Noise Performance of CMOS Amplifiers

1) CMOS amplifier

\[ A_{V1} = -g_{m1}(r_{ds1} || r_{ds2}) \]
\[ A_{V2} = -g_{m2}(r_{ds1} || r_{ds2}) \]

\[ g_{m1} = 2 \sqrt{\frac{\mu_{n} C_{ox}}{2} \frac{W_1}{L_1}} I_D \]
\[ g_{m2} = 2 \sqrt{\frac{\mu_{n} C_{ox}}{2} \frac{W_2}{L_2}} I_D \]

\[ e_n(IN) = \sqrt{\frac{a_{n1}}{W_1 L_1} \left[ 1 + \frac{\frac{\mu_{p} C_{ox}}{2} a_{n2}}{\mu_{n} C_{ox} 2 L_1} \right]^2} \]

Design considerations for low noise can be found.

2) CMOS differential-input to single-ended converter

\[ A_{V1} = \frac{1}{2} (g_{m1} + g_{m2}) (r_{ds1} || r_{ds2}) \quad \text{for} \quad e_{n1}, e_{n3} \]

\[ A_{V2} = g_{m2} (r_{ds1} || r_{ds2}) \]

If \( g_{m1} = g_{m3} \) and \( g_{m2} = g_{m4} \)

\[ \Rightarrow e_n(IN) = \sqrt{\frac{2 a_{n1}}{W_1 L_1} \left[ 1 + \frac{\frac{\mu_{p} C_{ox}}{2} a_{n2}}{\mu_{n} C_{ox} 2 L_1} \right]^2} \]

* \( W_1 \uparrow, L_2 \uparrow \Rightarrow e_n(IN) \downarrow \)

* Optimal \( L_1 = \sqrt{\frac{\mu_{p} C_{ox} 2}{2} a_{n1} L_2} \)

* The noise from \( M_2 \) and \( M_4 \) loads is very important!

Example: PMOS: \( \frac{\mu C_{ox}}{2} p = 3 \mu A / V^2 \)

\[ a_{np} = 48 \times 10^3 (\mu V \cdot \mu m)^2 \quad \text{for} \quad 20Hz \sim 20KHz \]

NMOS: \( \frac{\mu C_{ox}}{2} n = 7 \mu A / V^2 \)
\[ a_{uv} = 380 \times 10^3 (\mu V \cdot \mu m)^2 \text{ for } 20Hz \sim 20KHz \]

* NMOS is much more noisy than PMOS due to much larger \( \frac{1}{f} \) noise

Why? 1. Higher surface-state density
2. Nonuniform trap center distribution (more centers near conduction band)
3. Efficient electron trapping and releasing.

Bias current \( I_D = 5\mu A \), Gain \( \approx 44dB \)

Design 1: \( M_1, M_3 : \frac{500\mu m}{5\mu m} \) PMOS

\[ M_2, M_4 : \frac{100\mu m}{4\mu m} \text{ NMOS} \]

\[ \Rightarrow e_n(IN) = 38\mu V \text{ 20Hz} \sim 20KHz \]

(33.9)

Design 1: \( M_1, M_3 : \frac{500\mu m}{5\mu m} \) PMOS

\[ M_2, M_4 : \frac{50\mu m}{44\mu m} \text{ NMOS} \]

\[ \Rightarrow e_n(IN) = 7.5\mu V \text{ 20Hz} \sim 20KHz \]

(6.9)

3) CMOS inverter amplifier

\[ A_V = \frac{V_o}{V_i} = (g_{m1} + g_{m2})(r_{ds1} \parallel r_{ds2}) \]

\[ A_{V1} = -g_{m1}(r_{ds1} \parallel r_{ds2}) \text{ for } e_{n1} \]

\[ A_{V2} = -g_{m2}(r_{ds1} \parallel r_{ds2}) \text{ for } e_{n2} \]

\[ e_n(IN) = \sqrt{(g_{m1}e_{n1})^2 + (g_{m2}e_{n2})^2} \]

\[ \frac{g_{m1} + g_{m2}}{g_{m1} + g_{m2}} \]

If \( g_{m1} = g_{m2} \)

\[ \Rightarrow e_n(IN) = \frac{1}{2} \sqrt{e_{n1}^2 + e_{n2}^2} = \frac{1}{2} \sqrt{\frac{a_{n1}^2}{L_1} + \frac{a_{n2}^2}{L_2}} \]

* Larger size WL \( \Rightarrow \) smaller noise

If \( g_{m1} \neq g_{m2} \)
\[
\Rightarrow e_n (IN) = \sqrt{\frac{a_{ni}}{W_i L_1}} \left(1 + \frac{\left(\frac{\mu C_{ox}}{2}\right)_1 a_{ni} L_2^2}{\left(\frac{\mu p C_{ox}}{2}\right)_1 a_{ni} L_2^2} \right)
\]

* Increase the channel length of the transistor having the highest \(a_n\) parameter.

Example: Bias current 100\(\mu\) A

Design I: \(M_1: 1000\mu m / 5\mu m, M_2: 400\mu m / 4\mu m\)

\[\Rightarrow e_n (IN) = 8.1\mu V(7.97\mu V) \quad 20Hz \sim 20KHz\]

Design II: \(M_1: 1000\mu m / 5\mu m, M_2: 200\mu m / 8\mu m\)

\[\Rightarrow e_n (IN) = 5.9\mu V(5.65\mu V) \quad 20Hz \sim 20KHz\]

Design III: \(M_1: 500\mu m / 10\mu m, M_2: 400\mu m / 4\mu m\)

\[\Rightarrow e_n (IN) = 10.5\mu V(10.36\mu V)\]

* Best noise figure \(\Rightarrow\) highest \(\frac{W}{L}\) in PMOS

    lowest \(\frac{W}{L}\) in NMOS

Note: WL for PMOS (NMOS) are the same.


Noise spectrum of a typical MOSFET:

\[\text{\(\frac{V_{eq}^2}{(V^2/Hz)}\)}\]

\[\text{1/f noise}\]

\[\text{white noise}\]

\[\text{100} \quad \text{1K} \quad \text{10K} \quad \text{1M} \quad \text{10M}\]

\[\text{Frequency (Hz)}\]

§7-2.4 Noise performance of CMOS OP AMPS

1. Midband Analysis
Differential input stage

\[ \overline{V_{\text{nd}}}^2 = \overline{V_{n1}}^2 + \overline{V_{n2}}^2 + \left( \frac{g_{m4}}{g_{m1}} \right) (\overline{V_{n3}}^2 + \overline{V_{n4}}^2) \]

\[ \overline{V_{\text{ns}}}^2 = \overline{V_{n6}}^2 + \left( \frac{g_{m7}}{g_{m6}} \right)^2 \overline{V_{n7}}^2 \]

\[ \overline{V_n}^2 \approx \overline{V_{\text{nd}}}^2 + \frac{\overline{V_{\text{ns}}}^2}{A_d^2} = \overline{V_{n1}}^2 + \overline{V_{n2}}^2 + \left( \frac{g_{m4}}{g_{m1}} \right)^2 (\overline{V_{n3}}^2 + \overline{V_{n4}}^2) \]

\[ + \left[ \overline{V_{n6}}^2 + \left( \frac{g_{m7}}{g_{m6}} \right)^2 \overline{V_{n7}}^2 \right]/A_d^2 \]

* At low frequency \(<1\text{KHz}\), \(1/f\) noise dominates and \(|A_d(w)| >> 1\)

\[ \Rightarrow \overline{V_{\text{ns}}}^2 \] has a negligible effect on the OP noise.

The input stage dominates the overall noise contribution.

* At high frequency where \(|A_d(w)| = \frac{g_{m7}}{g_{m6}} \gg 1\), \(\therefore M_6, M_7\) is a level shifter, \(g_{m6}\) is small to obtain a large \(V_{Ga6} = \frac{g_{m7}}{g_{m6}} \gg 1\), the effect of \(V_{n7}\) is comparable to that of \(V_{n1}\) and \(V_{n2}\). Thus \(M_7\) must be a low-noise device (like PMOS).

The effect of \(V_{no}\) is negligible on the total equivalent input noise voltage since the gain of the gain stage is very high.

§7-2.5 High frequency analysis (for white noise)

For CMOS 2-stage OP AMP (without level shifter), the small-signal equivalent circuit is
(under unity-gain feedback)

\[
\frac{V_{out}}{V_{in1}} = \frac{A_V[1-s C_c \left( \frac{1}{g_{m2}} - R_z \right)]}{1 + A_V + as + b s^2 + cs^3}
\]

\[
\frac{V_{out}}{V_{in2}} = A_{V2} \left\{ 1 + s[C_c (R_1 + R_z) + C_1 R_1] + s^2 C_c C_c R_1 R_z \right\} \bigg( 1 + s C_c + s B s^2 C_c \bigg)
\]

when \( A_V = A_{V1} + A_{V2} \)

\[
a = C_c \left[ A_V \left( \frac{1}{g_{m1}} - \frac{1}{g_{m2}} - R_z \right) + R_1 + R_2 + R_z \right] + C_1 R_1 + C_2 R_2
\]

\[
b = R_1 R_2 (C_1 C_2 + C_1 C_c + C_2 C_c) + R_1 C_c (C_1 R_1 + C_2 R_2)
\]

\[
c = C_1 C_2 C_c R_1 R_2 R_z
\]

Usually, \(|A_V| >> 1\), \( R_z \ll R_1 \), \( R_z \ll R_2 \), \( C_1 \ll C_c \), \( C_1 \ll C_L \), and \( C_2 \ll C_L \)

\( \Rightarrow \) LHP Pole : \( P_1 = -\frac{g_{m1}}{C_c} \); \( P_2 = -\frac{g_{m2}}{C_L} \); \( P_3 = -\frac{1}{C_1 R_z} \)

RHP zero \( \left( \frac{V_{m1}}{V_{m2}} \right) \) : \( z_1 = \left[ C_c \left( \frac{1}{g_{m2}} - R_z \right) \right]^{\frac{1}{2}} \);

LHP zeros : \( -\frac{1}{C_1 R_1} = z_2 \), \( z_3 = -\frac{1}{C_1 R_2} \) \( (z_3 \rightarrow \infty) \)

If \( R_z = \frac{1}{g_{m2}} \) \( \Rightarrow z_1 = \infty \)

\( |z_2| < |P_1| < |P_2| \)

\( P_1 \approx -\frac{g_{m1}}{C_c} \); \( P_2 \approx -\frac{g_{m2}}{C_L} \); \( 1 \approx \frac{1}{A_P} \); \( 20 \text{dB/Dec} \)

\( 20 \text{dB/Dec} \)
The equivalent noise bandwidths are

\[ BW_1 = \frac{g_{ml}}{4C_c} \left( = \frac{|P_1|}{4} \right) \]

\[ BW_2 = \frac{g_{m2}}{4C_L} - \frac{g_{ml}}{4C_c} \left( = \frac{|P_2|}{4} - \frac{|P_1|}{4} \right) \]

\[ \Rightarrow \frac{g_{m2}}{4C_L} \quad (C_c >> C_L) \]

\[ \bar{\nu}_{\text{net}}^2 = \sum 4KT \gamma_i \frac{1}{g_{mi}} (BW_i) A_i, \quad \gamma_i = \text{cons tan t} \left( \approx \frac{3}{2} \right) \]

(Consider only thermal noise)

\[ = \frac{A_V}{1 + A_V} 4KT \gamma_1 \frac{1}{g_{ml}} \left( \frac{g_{ml}}{4C_c} \right) + \frac{A_{V2}'}{1 + A_V} 4KT \gamma_2 \frac{1}{g_{m2}} \left( \frac{g_{m2}}{4C_L} \right) \]

\[ = \frac{A_V}{1 + A_V} \gamma_1 \frac{KT}{C_c} + \frac{A_{V2}'}{1 + A_V} \gamma_2 \frac{KT}{C_L} \]

where \( A_{V2}' \) and \( A_V' \) are average gains between \( P_1 \) and \( P_2 \).

* The total white noise of the OP AMP is inversely proportional to \( C_c \) and \( C_L \).

* Due to the foldover effect in SCF, white noise (thermal noise) becomes important.

* 1) Clock feedthrough noise; 2) noises coupled from the power supplies, clock, and ground lines, and from the substrate; 3) white noise and flicker noise generated in the switches and OP AMPS are three major noise sources in the switched-capacitor circuits.

\section*{§7-2.6 Dynamic range of OP AMPS}

\( V_{\text{in, max}} \): the maximum input voltage which an OP AMP can handle without generating an excess amount of nonlinear distortion.

\( V_{\text{in, min}} \): the minimum input signal voltage which still does not drown in noise and distortion.

Dynamic range \( \equiv 20 \log_{10} \left( \frac{V_{\text{in, max}}}{V_{\text{in, min}}} \right) \)

For an open-loop OP AMP,
\[ V_{\text{in, max}} \approx V_c / A_d \]
\[ V_{\text{in, min}} \approx \sqrt{V_n} \]
\[ \Rightarrow \text{Dynamic range } \approx 30 - 40\text{dB}. \]

§7-3 Practical Design Consideration on Offset

§7-3.1 Input offset voltage of a CMOS OP AMP

1. Random offset \[ K \equiv \frac{C_o \mu}{2} \]

\[ V_{\text{os}} = V_{\text{gs}1a} - V_{\text{gs}1b} = \left[ \frac{2}{K_{\text{n}1a}} \left( \frac{L}{W} \right) I_{\text{a}} \right]^{\frac{1}{2}} - \left[ \frac{2}{K_{\text{n}1b}} \left( \frac{L}{W} \right) I_{\text{b}} \right]^{\frac{1}{2}} + V_{\text{th}1a} - V_{\text{th}1b} \]

\[ = \Delta V_{\text{th}1} + \left( \frac{2}{K_N} I_1 \right)^{\frac{1}{2}} \left[ \frac{L_1 + \frac{\Delta L}{2}}{W_1 + \frac{\Delta W}{2}} \right]^{\frac{1}{2}} - \left[ \frac{L_1 - \frac{\Delta L}{2}}{W_1 - \frac{\Delta W}{2}} \right]^{\frac{1}{2}} + \ldots \]

\[ = \Delta V_{\text{th}1} + \left( \frac{2}{K_N} I_1 \right)^{\frac{1}{2}} \left[ \frac{L_1 + \frac{\Delta L}{2}}{W_1 + \frac{\Delta W}{2}} \right]^{\frac{1}{2}} \left[ 1 - \frac{1}{2L_1} \right] \left[ 1 - \frac{1}{2W_1} \right] - \left[ \frac{L_1 - \frac{\Delta L}{2}}{W_1 - \frac{\Delta W}{2}} \right]^{\frac{1}{2}} \left[ 1 + \frac{1}{2L_1} \right] + \ldots \]

\[ = \Delta V_{\text{th}1} + \left( \frac{2}{K_N} I_1 \right)^{\frac{1}{2}} \left( \frac{\Delta L}{2L_1} - \frac{\Delta W}{2W_1} \right) - \left( \frac{2}{K_N} I_1 \right)^{\frac{1}{2}} \left( \frac{\Delta K_N}{2K_N} \right) + \left( \frac{2}{K_N} I_1 \right)^{\frac{1}{2}} \left( \frac{\Delta I}{2I_1} \right) \]

\[ A \equiv \frac{A_1 + A_2}{2} \quad \Delta A \equiv A_1 - A_2 \]
\[ \Delta I = I_{IA} - I_{IB} = \frac{K_{P3A}}{2} \left( \frac{W}{L} \right)_{J3A} (V_{GS3} - V_{TH3A})^2 - \frac{K_{P3B}}{2} \left( \frac{W}{L} \right)_{J3B} (V_{GS3} - V_{TH3B})^2 \]

\[ = K_p \frac{W_1}{L_3} (V_{GS3} - V_{TH3})^2 \left( \frac{\Delta K_p}{K_p} + \frac{\Delta W_3}{W_3} - \frac{\Delta L_1}{L_3} - \frac{2\Delta V_{TH3}}{V_{GS3} - V_{TH3}} \right) \]

\[ = I_{I_1} \left( \frac{\Delta K_p}{K_p} + \frac{\Delta W_3}{W_3} - \frac{\Delta L_1}{L_3} - \frac{2\Delta V_{TH3}}{V_{GS3} - V_{TH3}} \right) \]

\[ \Rightarrow V_{OS} = \Delta V_{TH1} + \left( \frac{2}{K_N} I_{I_1}, \frac{L_1}{W_1} \right) \left[ \frac{\Delta L_1}{2L_1} - \frac{\Delta W_1}{2W_1} - \frac{\Delta K_N}{2K_N} + \frac{\Delta K_p}{2K_p} + \frac{\Delta W_3}{2W_3} - \frac{\Delta L_2}{2L_2} - \frac{\Delta V_{TH3}}{V_{GS3} - V_{TH3}} \right] \]

\[ \approx \Delta V_{TH1} + \left( \frac{V_{GS1} - V_{TH1}}{2} \right) \left( \frac{\Delta W_3}{2W_3} + \frac{\Delta L_3}{2L_3} \right) - \left( \frac{K_p}{K_N} \right) \left( \frac{W_3}{W_1} \right) \Delta V_{TH3} \quad \text{(If} \frac{\Delta L_3}{2L_3}, \frac{\Delta W_3}{2W_3} \rightarrow 0 \text{)} \]

2). Systematic offset. \( V_{OS} = \frac{V_{Odc}}{A_O} \) where \( V_{Odc} \neq 0 \) and \( A_O \) is the dc gain of the OP AMP.

### 7-3-2 Low offset design techniques for CMOS OP AMPS

1. Layout techniques to reduce the random offset.

   a). linear variation of devices across a row of transistors or a matrix of transistors.

   ![Diagram](image1)

   or

   ![Diagram](image2)

   b). cross-coupled connection

   ![Diagram](image3)

   \( I_{DS} \propto V_{gs}^2 \cdot \frac{W}{L} \]

   \( L_{2B} = KL_{1B}, L_{2A} = KL_{1A}, \quad \frac{L_{1B}}{L_{1A}} = \frac{L_{2B}}{L_{2A}} = N, \quad \text{W’s are the same} \)

   Cross-coupled: \( I_{DS1A} + I_{DS1B} = I_{DS2A} + I_{DS2B} \)

   \[ \frac{V_{GS1}}{L_{1A}} + \frac{V_{GS1}}{L_{1B}} = \frac{V_{GS2}}{L_{2A}} + \frac{V_{GS2}}{L_{2B}} \Rightarrow \frac{V_{GS1}}{V_{GS2}} = \frac{1 + KN}{K + N} \]
If $K=1 \Rightarrow$ precision channel length control \( \Rightarrow \frac{V_{GS1}}{V_{GS2}} = 1 \Rightarrow \) Ordered dimension

error $\approx 0 \Rightarrow V_{OS} \approx 0$

If $K=1.1, \: N=1.1 \Rightarrow \frac{V_{GS1}}{V_{GS2}} = 1.0023$

But for single-pair design (1B, 2B, or 1A, 2A)

\( \frac{V_{GS1}}{V_{GS2}} = \sqrt{K} = \sqrt{1.1} = 1.049 \) larger $V_{GS}$ error $\Rightarrow$ larger $V_{OS}$


c) Common-centroid structures to reduce $\Delta V_{TH}$


2. General optimum matching rules to reduce the random offset

1. Same structure
2. Same temperature
3. Same shape, same size
4. Minimum distance
5. Common-centroid geometries
6. Same orientation
7. Same surroundings
8. Non minimum size


3. Low $V_{GS} - V_{TH1}$ to reduce the dimensional random offset

4. Dimension design to eliminate the systematic offset

\[
\frac{(W/L)_{3A}}{(W/L)_{3B}} = \frac{(W/L)_{3B}}{(W/L)_{4}} = \frac{1}{2} \Rightarrow \frac{(W/L)_{3A}}{(W/L)_{4}} \Rightarrow V_{oc} = 0 \Rightarrow \text{systematic offset} \approx 0
\]

To avoid the process-induced variations in channel lengths, we usually choose $L_{4} = L_{3A} = L_{3B}$.

But this design will enhance the noise contribution from the PMOS $M_{3A}, M_{3B}$ (NMOS $M_{3A}, M_{3B}$ for PMOS-input structure).

$\Rightarrow$ A compromise is required.

5. Sample-data techniques to eliminate the offset voltage.

Ref.: IEEE JSSC, p.499, Aug. 1978

IEEE JSSC, pp.837-844, Aug. 1985

Applications: Zero-offset OP AMPS, High-precision comparators,
Instrumentation amplifiers, High-precision amplifiers,
Switched-capacitor amplifier, Switched-capacitor network.
1) Offset cancellation in OP-AMP-based switched-capacitor (SC) amplifier

(1) SC amplifier

\[ V_{in} \alpha C + V_{os} = V_o \]

\[ \Rightarrow V_o = \alpha + \frac{V_{os}}{V_{in}} \]

(2) Modified SC Amplifier

Step 1: Switch 1 ON, Switch 2 OFF:

Step 2: Switch 2 ON, Switch 1 OFF:
*The charge injection error of the switched S1 cannot be eliminated.

2) Offset cancellation in precision amplifier

Switch:

\[ C_s : \varepsilon = \frac{10^V}{0.1pF} \frac{C_p}{C_p + C_s} \]

\[ C_s = 10nF \]

\[ \Rightarrow \varepsilon = 10^V \frac{0.1pF}{0.1pF + 10000pF} = 100\mu V \]

\[ C_s \uparrow \varepsilon \downarrow \]

or using the differential outputs rather than the single output to eliminate the common mode voltage \( \varepsilon \)

RSM amplifier (P-MOSFETs)

* amplifier with offset voltage memorization
* residual voltage successive memorization (RSM) amplifier
* auto-zero design
* chopper-stabilized design

※ capable of reducing the offset voltage by 1~4 order of magnitude
$V_{off} = (e_n + \varepsilon_n) / G_1 G_2 \cdots G_{n-1}$

$e_n$ : input offset voltage

$\varepsilon_n$ : parasitic clock error pulse of the $n$th stage
§8-1 Advanced Design Techniques of CMOS OP AMPS

§8-1.1 Improved PSRR and frequency compensation

\[
\frac{\partial V_{\text{out}}}{\partial V_{ss}} \approx \frac{C_{gs}}{C_I} \left[ \frac{\partial I_o}{\partial V_{ss}} \frac{1}{2g_{m1}} + \frac{\partial V_{GS1}}{V_{ss}} \right] + \frac{C_{gd}}{C_I} \frac{1}{2g_{m3}} \frac{\partial I_o}{\partial V_{ss}}
\]

\[
\frac{\partial V_{\text{out}}}{\partial V_{DD}} \approx \frac{C_{gd}}{C_I} \left[ 1 - \frac{\partial I_o}{\partial V_{DD}} \frac{1}{2g_{m3}} \right] + \frac{C_{gs}}{C_I} \frac{1}{2g_{m1}} \frac{\partial I_o}{\partial V_{DD}}
\]

Where \( I_o \) represents the input stage bias current.

If \( I_o \) is independent of \( V_{ss} \) and \( V_{DD} \) and the input devices have no body effect.

\[
\Rightarrow \quad \frac{\partial V_{\text{out}}}{\partial V_{ss}} \to 0 \quad \frac{\partial V_{\text{out}}}{\partial V_{DD}} \to -\frac{C_{gd}}{C_I}
\]


BIAS GENERATOR

\* \( I_{REF} \) is generated by using the power supply independent current source.

\* \( V_{BIAS} \) is nearly independent of \( V_{DD} \) and \( V_{ss} \).

\* It is better to use separate p-wells for \( M_1 \) and \( M_2 \) to avoid the body effect.
Tracking RC compensation

Conceptual circuits:

In the quiescent case, $V_{in2} = V_{OS2}$  

If \((W/L)_A = [(W/L)_B \cdot (W/L)_C]^{1/2}\)  

\[
R_{dA} = \frac{C_c + C_L}{g_{m2} C_c} = R_c
\]

Thus LHP zero = LHP pole P2  
and P3 becomes the second pole.

The stability considerations,  

\[
P_3 \geq A_{dc} P_1
\]

or  

\[
C_c \geq \sqrt{\frac{g_{m1}}{g_{m2}} c_c c_L}
\]

allows a smaller $g_{m2}$ and larger $C_L$  

* $R_{dA} = R_c$ indep of temperature, process, and supply variations.  

=> Tracking design to make sure that $z = P_2$  
=> No pole-zero doublet problem!
* M17, Cc: Tracking RC compensation.
* M9, M11: Sharing the separate n-well.
* $V_{\text{BIAS}}$ is not strictly independent of $V_{\text{DD}}$ and $V_{\text{SS}}$.

§8-1.2 Improved frequency compensation technique.
Grounded gate cascode compensation
MB, Cgs: low pass filter for high frequency noises.
M8, M9, M10: new compensation circuit.
M11~M16: Bias generator.

Conceptual circuits:

Net current in $C_c \ (C_c \frac{d}{dt} V_o)$ enters the second stage.

The input voltage $V_i$ can’t reach the node $A$
- Better PSRR ($\n$ no low-freq. zero $\n$, especially PSRR
- Allow larger capacitive loads.
- Slight increase in complexity, random offset and noise.

§ 8-1.3 Improved cascode structure
1. To improve gain:
* Substantial reduction in input-stage common-mode range.
* Improved wilson current source is used as the load to improve the balance of the first stage.

2. Single-stage push-pull class AB CMOS OP AMP
   * Inverting mode only. (+ grounded)
   * Capable of high current driving and high voltage gain.
   * Not a differential-amplifier-based OP AMP.

3. Cascoded CMOS OP AMP with high ac PSRR
      (2) IEEE JSSC, vol SC-19, pp. 919-925, Dec. 1984

1) Original version

Characteristics:

\[ V_{DD} = V_{SS} = 2.5V \]
Input offset voltage \( 5mV \)
Supply current \( 100\mu A \)
Output voltage range \( -V_{SS} - V_{DD} \)
Input common mode range \( -V_{SS} + 1.47V \sim V_{DD} \)
CMRR @ 1KHz \( 99\text{dB} \)
Unity-gain frequency \( 1.0\text{MHz} \)
Slew rate \( 1.8 \text{ V/μsec} \)
* Better input common-mode range.
* Vic $\Rightarrow V_{DSN4} \Rightarrow I_{DSN4} \Rightarrow V_A \Rightarrow M_{N8}$ is turned on $\Rightarrow V_{out} \Rightarrow -V_{SS}$
  voltage spike at $V_{out}$.
* The possible spike in the settling period.

2) Improved version

![Circuit Diagram](image1)

* $M_{12}, M_{13}$ and $M_{14}$: Let the drain bias currents of $M_{10}$ and $M_{11}$ follow the change of $I_{D7}$ under positive input common mode voltage.
  $\Rightarrow$ No voltage spike at $V_{out}$
  Also serves as CMFB
* Better PSRR and input common-mode range.
* $C_c$ is decoupled from the gate of the driver $M_8$.

4. Simple cascoded CMOS OP AMP


![Circuit Diagram](image2)

* Good PSRR
* Reduced input common range.
  $\Rightarrow$ restrict its applications to those which use a virtual ground.
5. Single-stage cascode OTA


$T_9, T_{10}$: Cascode structure

* Output conductance $\downarrow$ without any noise penalty and with only a very small reduction of phase margin.

$\Rightarrow$ Gain $\uparrow$ no any compensation is necessary.

* Maximum output swing $\downarrow$

§ 8-2 Advanced Design Techniques on High-frequency Non-differential-type CMOS OP AMPs

1. Single-ended push-pull CMOS OP AMP

*Current-gain-based design
### TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-Open Circuit Gain</td>
<td>69dB</td>
</tr>
<tr>
<td>Unity0Gain Bandwidth</td>
<td>70MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>40°</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>200 V/µsec</td>
</tr>
<tr>
<td>PSRR (DC+)</td>
<td>68dB</td>
</tr>
<tr>
<td>PSRR (DC-)</td>
<td>66dB</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>10mV</td>
</tr>
<tr>
<td>CMRR (DC)</td>
<td>62dB</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>1.5 $V_p$</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>3 $M\Omega$</td>
</tr>
<tr>
<td>Input Referred Noise (@1KHz)</td>
<td>0.54 $\mu V/ \sqrt{Hz}$</td>
</tr>
<tr>
<td>DC-Power Dissipation</td>
<td>1.1mWatt</td>
</tr>
</tbody>
</table>

$V_{DD} = +3V$ ; $V_{cc} = -3V$ ; $I_{B1} = 50\mu A$ ; CL=1pF

### TABLE II

<table>
<thead>
<tr>
<th>Bias Current</th>
<th>Unity-Gain Bandwidth</th>
<th>DC-Open Circuit Voltage Gain</th>
<th>DC-Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 $\mu A$</td>
<td>50MHz</td>
<td>70dB</td>
<td>0.55mW</td>
</tr>
<tr>
<td>50 $\mu A$</td>
<td>70MHz</td>
<td>69dB</td>
<td>1.1mW</td>
</tr>
<tr>
<td>100 $\mu A$</td>
<td>100MHz</td>
<td>66dB</td>
<td>2.2mW</td>
</tr>
</tbody>
</table>
\[ V_{DD} = +3V \quad V_{CC} = -3V \quad CL=1pF \]

2. Low output resistance CMOS OP AMP
   * \( C_L \) is a compensation capacitor
   * For low-resistance load
   * Smaller maximum output voltage swing.
   * \( I_{BI} = 50\mu A, C_L = 1pF \), \( f_u = 60MHz \)

§ 8-3 Advanced Design Techniques on High-drive MOS Power or Buffer OP AMPS

§ 8-3.1 Efficient Output Stages.

A. CMOS output stage using a bipolar emitter follower and a low-threshold PMOS source follower.
B. Complementary class B output stage using compound devices with common-source output MOS.

\[ V_{out} = +V_{DD} \]
\[ V_{i} \to M_{P} \to V_{out} \]
\[ V_{i} \to M_{N} \to -V_{SS} \]

§ 8-3.2 High-drive power or buffer CMOS OP AMPs

1. Large swing CMOS power amplifier (National Semiconductor)
* Noninverting unity gain amplifier

\[ V_{in} \equiv V_{out} \]

M_6 provides the negative feedback

* A_1, M_6, and A_2, M_{6A} form a class AB push-pull output stage.

* Full swing from +V_{DD} to -V_{SS}

* M_9, M_{10}, M_{11}, and M_{12} form a current feedback to stabilize the bias current of M_6 and M_{6A}.

Offset in A_1, e.g. \( V_{mA1}^- \uparrow \Rightarrow V_{outA1} \downarrow \Rightarrow I_{DM6} \uparrow \) and \( I_{DM9} \uparrow \Rightarrow I_{DM11} \uparrow \)

and \( I_{DM12} \uparrow \Rightarrow V_{GS8A} \uparrow \) and \( V_{mA2}^+ \downarrow \Rightarrow V_{out} \uparrow \), i.e.

\( V_{mA1}^+ \uparrow \Rightarrow V_{out} \downarrow \Rightarrow V_{mA1}^- \downarrow \) (virtual short between + and -) \( \Rightarrow V_{mA2}^- \downarrow \) through \( M_8 \Rightarrow \) All the bias voltage and current are restored to the normal values and the offset is absorbed by \( M_{8A} \).

Since the current feedback is not unity gain, some current variation in transistors M_6 and M_{6A} still exists.
Large positive common mode range allows \( M_6 \) to source large amount of current to the load. (because \( V_{in} \equiv V_{out} \))

The maximum \( V_{GS6} \) which \( M_1 \) and \( M_2 \) still in the saturation region is

\[
V_{GS6\,\text{max}} = -(V_{DD} - (V_{IN} - V_{GS1} + V_{DSAT1})) = -(V_{CC} - V_{IN} + V_{TH1})
\]

\[\Rightarrow V_{TH1} \uparrow \Rightarrow V_{GS6\,\text{max}} \uparrow \Rightarrow I_{DM6} \uparrow\]

(1). Threshold implant to increase \( V_{THO1} \)

(2). Negative substrate bias \( -V_{SS} \) to increase \( V_{TH1} \)

* The input stage is not shown in the diagram.

* \( M_{16}, M_8, M_{17} \) form the second stage with \( C_D \) the Miller compensation capacitor.

* If \( V_{out} \rightarrow -V_{SS}, V_{DSM5} \rightarrow 0 \) and \( I_{DSM5} \rightarrow 0 \).

\[\Rightarrow M_1, M_2, M_3 \text{ and } M_4 \text{ are off}\]

\[\Rightarrow M_{3H} \text{ and } M_{4H} \text{ are still on to keep } V_{GS6} \equiv 0V.\]

Otherwise , \( M_6 \) will be turned on.

Similarly, \( M_{3HA} \) and \( M_{4HA} \) turn off \( M_{6A} \) in the positive voltage swing

* \( M_{P3}, M_{N3}, M_{N4}, M_{P4} \) and \( M_{P5} \) are output short-circuit protection circuitry.

Normally, \( M_{P5} \) is off.
When \( I_{DM6} \equiv 60\text{mA} \), \( I_{DM3} \uparrow \Rightarrow I_{DMN4} \uparrow \Rightarrow V_{GSMP5} \uparrow \).

\[ \Rightarrow I_{DM6} \] is limited to approximately 60 mA.

**Table I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation</th>
<th>Measured Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power dissipation(( \pm 5V ))</td>
<td>7.0mW</td>
<td>5.0mW</td>
</tr>
<tr>
<td>( A_{vol} )</td>
<td>82dB</td>
<td>83dB</td>
</tr>
<tr>
<td>( F_u )</td>
<td>500KHz</td>
<td>420KHz</td>
</tr>
<tr>
<td>( V_{offset} )</td>
<td>0.4mV</td>
<td>1mV</td>
</tr>
<tr>
<td>PSRR+(dc) ((1\text{KHz}))</td>
<td>85dB</td>
<td>86dB</td>
</tr>
<tr>
<td>PSRR-(dc) ((1\text{KHz}))</td>
<td>104dB</td>
<td>106dB</td>
</tr>
<tr>
<td>THD ( V_{IN}=3.3V_p ) ( R_L=300\Omega ) ( C_L=1000\text{pF} )</td>
<td>0.03%</td>
<td>0.13%(1\text{KHz})</td>
</tr>
<tr>
<td></td>
<td>0.08%</td>
<td>0.32%(4\text{KHz})</td>
</tr>
<tr>
<td>THD ( V_{IN}=4.0V_p ) ( R_L=15\text{k}\Omega ) ( C_L=200\text{pF} )</td>
<td>0.05%</td>
<td>0.13%(1\text{KHz})</td>
</tr>
<tr>
<td></td>
<td>0.16%</td>
<td>0.20%(4\text{KHz})</td>
</tr>
<tr>
<td>( T_{setting} ) (0.1%)</td>
<td>3.0us</td>
<td>&lt;5.0us</td>
</tr>
<tr>
<td>Slew rate</td>
<td>0.8V/us</td>
<td>0.6V/us</td>
</tr>
<tr>
<td>1/f noise at 1KHz</td>
<td>N/A</td>
<td>130nV/\text{Hz}</td>
</tr>
<tr>
<td>Broad-band noise</td>
<td>N/A</td>
<td>49nV/\text{Hz}</td>
</tr>
<tr>
<td>Die area</td>
<td></td>
<td>1500\text{mils}^2</td>
</tr>
</tbody>
</table>

**Table II**

| COMPONENT SIZES (\( \mu \text{m} \text{, pF} \)) |
|-----------------------------------------------|---|---|
| 8 - 13 CHUNG-YU WU                          | 8 - 14 CHUNG-YU WU |
Maximum loads : 300Ω and 1000pF to ground.


2. High-performance CMOS power amplifier (Siemens AG)

(1). New input stage : 3 gain stages.

* Cc is connected to the source of $M_9$ to improve PSRR
* Three poles and one zero:

\[
Z = \frac{-2g_{m6}g_{m8}g_{m13}}{C_c g_{m6} g_{m13} + C_1 g_{m8} g_{m12}} \text{ LHP.}
\]

\[
P_1 = \frac{-g_{d10}g_{o}}{g_{m13}C_c}
\]

\[
P_2, P_3 = \frac{-g_{m5}(C_c + C_O)}{2C_c C_o} \pm \frac{g_{m8}g_{m13}}{C_O C_1} \left[ \frac{g_{m8}(C_O + C_c)}{2C_c C_c} \right]^{1/2}
\]

where \( g_{o} \equiv g_{d12} + g_{d13} \)

\( C_O = C_k + C_{db12} + C_{db13} \)

\( C_1 = C_{gd13} + C_{db11} + C_{db9} + C_{gd9} \)

Design guidelines for stability:

\( g_{m8} \) large, \( g_{m13} \gg g_{m6} \)

(2) Output stage

Class AB source follower

* One pole and one zero at high frequencies.

* Not full swing
Pseudo source follower

* The quiescent current in $M_1$ and $M_2$ will vary widely with variations in $V_{os1}$ and $V_{os2}$.
* Suitable common-mode range of the two amplifiers $A_1$ and $A_2$ are required.
* Large phase shift at high frequencies due to $A_1$ and $A_2$ $\Rightarrow$ stability problem.

Combined output stage:

* $M_1$ and $M_2$ are turned off in the quiescent state by building a small offset voltage into $A_1$ and $A_2$ $\Rightarrow M_3$-$M_6$ control the output quiescent currents.
* $M_2$($M_1$) sinks (sources) approximately 95% of the required currents.
* $M_1$ and $M_2$ provide a high-frequency feed-forward path.

Still has a smaller swing limited by $M_5$, $M_6$. 
* M_{13}, M_{14} and M_{15} form a circuit to turn off M_{15} when V_{out} < V_{TP13} (negative)

* $C_c$: compensation.

* Three poles and one zeros.

$$Z_1 = -\frac{g_{m7} + g_{mbs7}}{C_c + C_{gs7}}$$

$$P_1 = \frac{-g_L}{C_L + C_c \frac{g_{m15}}{g_{ds6}}}$$

$$P_2, P_3 = -\frac{g_{m7}(C_c + C_L)}{2C_cC_L} \pm j \frac{g_{m7}g_{ds6}(C_c + C_{gs6}) + \frac{g_{m7}}{g_{ds6}}}{C_cC_LC_1} - \left(\frac{g_{m7}(C_c + C_L)}{2C_cC_L}\right)^{1/2} \text{ where}$$

$$C_1 = C_{gs9} + C_{db6} + C_{db7} + C_{gd7}$$
TABLE I  Component Sizes

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>400/15</td>
<td>MH1</td>
</tr>
<tr>
<td>M2</td>
<td>400/15</td>
<td>MH2</td>
</tr>
<tr>
<td>M3</td>
<td>150/10</td>
<td>MH3</td>
</tr>
<tr>
<td>M4</td>
<td>150/10</td>
<td>MH4</td>
</tr>
<tr>
<td>M5</td>
<td>100/15</td>
<td>MH5</td>
</tr>
<tr>
<td>M6</td>
<td>150/10</td>
<td>MH6</td>
</tr>
<tr>
<td>M7</td>
<td>150/10</td>
<td>MH7</td>
</tr>
<tr>
<td>M8</td>
<td>300/5</td>
<td>MH8</td>
</tr>
<tr>
<td>M9</td>
<td>300/5</td>
<td>MH9</td>
</tr>
<tr>
<td>M10</td>
<td>300/10</td>
<td>MH10</td>
</tr>
<tr>
<td>M11</td>
<td>300/10</td>
<td>MH11</td>
</tr>
<tr>
<td>M12</td>
<td>1200/10</td>
<td>Cc1</td>
</tr>
<tr>
<td>M13</td>
<td>600/10</td>
<td>Cc2</td>
</tr>
<tr>
<td>M14</td>
<td>200/5</td>
<td>Cc3</td>
</tr>
<tr>
<td>M15</td>
<td>200/5</td>
<td></td>
</tr>
<tr>
<td>M16</td>
<td>600/6</td>
<td></td>
</tr>
<tr>
<td>M17</td>
<td>600/6</td>
<td></td>
</tr>
</tbody>
</table>
### TABLE II  
POWER AMPLIFIER PERFORMANCE SUMMARY  
(First Revision)

<table>
<thead>
<tr>
<th>parameter</th>
<th>Measured Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplies</td>
<td>±5V</td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td>93dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1.2MHz</td>
</tr>
<tr>
<td>Power Dissipation x</td>
<td>12.7 mW</td>
</tr>
<tr>
<td></td>
<td>1.76mW</td>
</tr>
<tr>
<td>Output Swing (R&lt;sub&gt;L&lt;/sub&gt;=200Ù)</td>
<td>±3.1V</td>
</tr>
<tr>
<td>PSRR+ at DC</td>
<td>93dB</td>
</tr>
<tr>
<td>1 kHz</td>
<td>91dB</td>
</tr>
<tr>
<td>10 kHz</td>
<td>76dB</td>
</tr>
<tr>
<td>100 kHz</td>
<td>60dB</td>
</tr>
<tr>
<td>PSRR- at DC</td>
<td>102dB</td>
</tr>
<tr>
<td>1 kHz</td>
<td>89dB</td>
</tr>
<tr>
<td>10 kHz</td>
<td>75dB</td>
</tr>
<tr>
<td>100 kHz</td>
<td>53dB</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>1.5V/ìs</td>
</tr>
<tr>
<td>Input Common Mode Range</td>
<td>+3.3V</td>
</tr>
<tr>
<td></td>
<td>-5.5V</td>
</tr>
<tr>
<td>Die Area (5ì m CMOS)</td>
<td>1000 mils²</td>
</tr>
<tr>
<td>Harmonic Distortion (3 kHz)</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;m&lt;/sub&gt;=3 V&lt;sub&gt;p&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;L&lt;/sub&gt;=200Ù</td>
<td></td>
</tr>
<tr>
<td>HD2</td>
<td>-73dB</td>
</tr>
<tr>
<td>HD3</td>
<td>-78dB</td>
</tr>
</tbody>
</table>

Maximum Loads : 1000pF and 200Ù to ground.

3. Efficient Unity-gain CMOS buffer for driving large $C_L$.

High-drive OTA buffer

```
TABLE I
TRANSISTORS’ DIMENSIONS

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>W (µm)</th>
<th>L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MX1, MX5</td>
<td>225</td>
<td>3</td>
</tr>
<tr>
<td>MX2</td>
<td>75</td>
<td>3</td>
</tr>
<tr>
<td>MX3</td>
<td>30</td>
<td>3</td>
</tr>
<tr>
<td>MX4, MX6</td>
<td>90</td>
<td>3</td>
</tr>
<tr>
<td>MR1</td>
<td>6</td>
<td>21</td>
</tr>
<tr>
<td>MA1, MA4</td>
<td>45</td>
<td>3</td>
</tr>
<tr>
<td>MA2, MA3</td>
<td>450</td>
<td>3</td>
</tr>
<tr>
<td>MA5</td>
<td>36</td>
<td>3</td>
</tr>
<tr>
<td>MX7</td>
<td>600</td>
<td>3</td>
</tr>
<tr>
<td>MX8</td>
<td>240</td>
<td>3</td>
</tr>
</tbody>
</table>
```

- * $M_{R1}$ has a low $W/L$ and is operated in the linear region
  ⇒ like a linear resistor.
- * $M_{X2}$ and $M_{X3}$

Quiescent operation:

- $M_{X2}$ and $M_{X3}$ are on.

⇒ $V_{GSMX7}$ and $V_{GSMX8}$ low to reduce dc power.
⇒ Provide a low-impedance level at node A and B.

The low-order poles created by the Miller cap. of MX7 and MX8 can be avoid

* IfVin << 0

MX3-MX6 are turned off and MX1 and MX2 are on
⇒ Node A has a high voltage ⇒ MX7 off.

VB = VA because of MR1 ⇒ MX8 on.

* In the bias circuit, MR2 ↔ MB1, MB1 ↔ MX1, MB2 ↔ MX2, MB3 ↔ MX3, MB4 ↔ MX4.

In the quiescent case, VGSMX1 ≈ VGSMX7 and VGSMX4 ≈ VGSMX8
⇒ The current in MB1 and MB4 controls that in MX1 and MX4 and MX7 and MX8.

* RBIAS controls the current through MB2 and MB3.
⇒ i.e. the current through MX2 and MX3.

Characteristics:

3 μm CMOS area: 100mils².

CL ≥ 100pF and RL ≥ 10 kΩ : stable.

CL=5000pF ⇒ f ≈ 100kHz.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MEASURED VALUE</th>
<th>SPICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>± 2.5 V</td>
<td>± 2.5 V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>285 μA</td>
<td>270 μA</td>
</tr>
<tr>
<td>Voffset</td>
<td>&lt; 10 mV</td>
<td>5 mV</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>+ 1.00 V/V</td>
<td>+ 1.00 V/V</td>
</tr>
<tr>
<td>F3dB (CL=100pF)</td>
<td>6 MHz</td>
<td>8 MHz</td>
</tr>
<tr>
<td>Gain Peaking</td>
<td>0.4 dB</td>
<td>0</td>
</tr>
<tr>
<td>RCL</td>
<td>330 Ω</td>
<td>270 Ω</td>
</tr>
<tr>
<td>CMRR</td>
<td>80 dB</td>
<td>84 dB</td>
</tr>
<tr>
<td>Input CM Range</td>
<td>± 1.8 V</td>
<td>± 1.7 V</td>
</tr>
<tr>
<td>SR (CL=5nF)</td>
<td>± 0.9 V/μs</td>
<td>± 1.0 V/μs</td>
</tr>
<tr>
<td>Tsettling (to 1%)</td>
<td>3.9 μs</td>
<td>4 μs</td>
</tr>
</tbody>
</table>
§ 8-4 Advanced Design Techniques on Fully differential type CMOS OP AMPS

1. Low-noise chopper-stabilized OP AMP

   Techniques for the reduction of 1/f noise:

   1) Use large device geometries.
      Possibly too large chip area.

   2) Use buried channel devices
      Not a standard technology.

   3) Transform the noise to a higher frequency range
      So that it does not contaminate the signal.
      a. The correlated double sampling (CDS) method
      b. The chopper stabilization method

   a. CDS method

   \[ V_{\text{IN}} \quad \sum \quad V_{\text{OUT}} \]

   \[ S/H \]

   \[ V_{\text{IN}2} \quad V_{\text{OUT}} \]

   \[ \Rightarrow \text{Noise reduction} \]

   b. Chopper stabilization method
If the chopper frequency is much higher than the signal bandwidth, the 1/f noise in the signal band will be greatly reduced.

Example: Fully differential class AB chopper stabilized OP AMP with DCMFB circuit.

Major advantage of fully differential OP AMPs:

1. Improvement of PSRR
2. Improvement of dynamic range
3. Double the output swing
4. Reduction on the sensitivity to clock and supply noise.

Disadvantage:
1. Larger area, mainly due to interconnection
2. Additional design complexity
3. Increase power dissipation.

M43-M46, M47-M54: the input chopper and the output chopper.
M29-M42, C1-C4: DCMFB circuit

<table>
<thead>
<tr>
<th>Device</th>
<th>W(um)</th>
<th>L(um)</th>
<th>Device</th>
<th>W(um)</th>
<th>L(um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>25</td>
<td>3</td>
<td>M19</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td>M2</td>
<td>25</td>
<td>3</td>
<td>M20</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td>M3</td>
<td>25</td>
<td>3</td>
<td>M21</td>
<td>17.5</td>
<td>3.5</td>
</tr>
<tr>
<td>M4</td>
<td>25</td>
<td>3</td>
<td>M22</td>
<td>17.5</td>
<td>3.5</td>
</tr>
<tr>
<td>M5</td>
<td>25</td>
<td>3</td>
<td>M23</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td>M6</td>
<td>25</td>
<td>3</td>
<td>M24</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td>M7</td>
<td>25</td>
<td>3</td>
<td>M25</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>M8</td>
<td>25</td>
<td>3</td>
<td>M26</td>
<td>3.5</td>
<td>3.5</td>
</tr>
</tbody>
</table>
2. Fully differential folded cascode amplifier (National Semiconductor)

For internal OP AMPs, high output impedance is O.K.

⇒ simple 2-stage or single-stage OP AMP.

![Two-Stage and Single-Stage Amplifiers Diagram]

**TWO-STAGE**

**SINGLE-STAGE**

**CASCODE**

**DOMINANT AND NONDOMINANT POLE LOCATIONS FOR THE TWO-AND SINGLE-STAGE AMPLIFIERS**

<table>
<thead>
<tr>
<th></th>
<th>Dominant pole location</th>
<th>Nondominant pole location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two-stage amplifier</td>
<td>( \frac{1}{r_C g_m r_o} )</td>
<td>( \frac{g_m}{C_L} )</td>
</tr>
<tr>
<td>One-stage amplifier</td>
<td>( \frac{1}{r_f C_L g_m r_o} )</td>
<td>( \frac{g_m}{C_p} )</td>
</tr>
</tbody>
</table>

In general, the higher the 2\(^{nd}\) pole frequency, the faster the settling response.

⇒ Single-stage cascode amp. has a faster settling behavior.
CMFB: Common-mode feedback circuitry

3. High-performance micropower fully differential OP AMP.

Simplified schematic of the class AB amplifier:
Active portion of the amplifier for a positive input signal.

Detailed schematic of the entire amplifier without CMFB:
NMOS dynamically biased current mirror:

If $I_9 = I_{30}$, $V_{GS9} = V_{GS13} = V_{GS15}$

$$V_{DS13} = V_{GS30} - V_{GS9}$$

Set $V_{DG13} = -V_{TH} \Rightarrow V_{GS30} = 2V_{GS9} - V_{TH}$

Design $(\frac{W}{L})_{30}$, such that $V_{GS30} = 2V_{GS9} - V_{TH}$

$\Rightarrow M_{13}$ is always sat. at the edge of the linear region.

$\Rightarrow$ Output swing↑

* Dynamic CMFB is used.
| M11 | 29 | 7 |
| M12 | 29 | 7 |
| M13 | 22 | 10 |
| M14 | 29 | 7 |
| M15 | 22 | 6 |
| M16 | 29 | 6 |
| M17 | 29 | 7 |
| M18 | 22 | 10 |
| M19 | 22 | 6 |
| M20 | 29 | 6 |
| M21 | 20 | 9 |
| M22 | 6  | 12 |
| M23 | 28 | 6 |
| M24 | 6  | 14 |
| M25 | 20 | 9 |
| M26 | 6  | 12 |
| M27 | 28 | 6 |
| M30 | 6  | 14 |

**AMPLIFIER SPECIFICATIONS**

**CORE AMPLIFIER SPECIFICATIONS**

(0-5 Volts Supply)

100 µW Quiescent Power Dissipation

<table>
<thead>
<tr>
<th>DIFFERENTIAL GAIN</th>
<th>&gt;10.000*</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNITY GAIN FREQUENCY</td>
<td>2 MHz*</td>
</tr>
<tr>
<td>NOISE</td>
<td>140 nV/√Hz 1KHz</td>
</tr>
<tr>
<td>OUTPUT SWING</td>
<td>50 nV/√Hz white</td>
</tr>
<tr>
<td>AREA</td>
<td>300 mils²</td>
</tr>
</tbody>
</table>

* inferred from filter measurement

4. Fully differential class AB OP AMP with CMFB circuit

Characteristics:

Technology : 5um, P-well CMOS, double-poly cap.
Open loop gain : 1180  unity-gain freq : 10Mhez
CMRR : 61db  power consumption : 2.3mw
Area : 290 mils$^2$  power supply : $\pm 5V$

Ref: IEEE JSSC ,vol.sc-20 , pp.1103-1112 , Ddec,1985
§ 8-5 Recent Design Examples of CMOS OP Amps

§ 8-5.1 Fast-settling CMOS OP AMP for SC Circuit with 90-dB DC Gain


1. Gain boosting
   1) Cascode gain stage with gain enhancement

\[ R_{out} = [g_{m2}r_{o2}(A_{add} + 1) + 1]r_{o1} + r_{o2} \]
\[ A_{tot} = g_{m1}r_{o1}[g_{m2}r_{o2}(A_{add} + 1) + 1] \]
\[ A_{orig} = g_{m1}g_{m2}r_{o1}r_{o2} \]

2) Repetitive implementation of gain enhancement

2. High-frequency behavior
We want $\omega_{4} = \omega_{5}$

$\omega_{2} > \omega_{1} \Rightarrow$ The bandwidth is determined by $\omega_{1}$, i.e. $R_{\text{out}}$ and $C_{\text{load}}$.

$\Rightarrow \omega_{4} > \omega_{3}$

But $\omega_{4} < \omega_{5}$ for easy design of $A_{\text{add}}$.

$A_{\text{add}}$ and M2 forms a close loop with the dominant pole of $\omega_{2}$ and the second pole at the source of M2, i.e. $\omega_{6}$

The stability consideration requires $\omega_{4} < \omega_{6}$

$\Rightarrow$ The safe range of $\omega_{4}$ is $\omega_{3} < \omega_{4} < \omega_{6}$

* The repetitive usage of the gain-enhancement techniques yields a decoupling of the op-amp gain and unity-gain frequency $f_{u}$. That is: gain↑ without $f_{u}$ ↓.

3. Settling behavior

1. Total output impedance $Z_{\text{tot}}$

$$Z_{\text{tot}} = \frac{Z_{\text{load}}}{Z_{\text{out}}}$$

$Z_{\text{load}}$: impedance of $C_{\text{load}}$

$Z_{\text{out}}$: output impedance of the amplifier

$Z_{\text{tot}} \equiv Z_{\text{orig}} (\text{Add}+1)$
\[ \omega_2 : \text{Upper-3dB freq. of } A_{\text{add}} \]

\[ \Rightarrow \text{the same for } Z_{\text{out}} \]

\[ \omega_4 : \text{Unity-gain freq. of } A_{\text{add}} \]

For \( \omega > \omega_4 \), \( A_{\text{add}} < 1 \) \( \Rightarrow Z_{\text{out}} \rightarrow Z_{\text{orig}} \)

\[ \Rightarrow \text{A zero is formed at } \omega_4 \text{ for } Z_{\text{out}} \]

\[ Z_{\text{total}} = Z_{\text{load}} \parallel Z_{\text{out}} \Rightarrow \text{A pole-zero doublet is formed around } \omega_4 \]

\[ \Rightarrow \text{The same doublet of } A_{\text{total}} \]

3. Design technique for fast settling

The time constant of the doublet, \( \frac{1}{\omega_{PZ}} \), must be smaller than the main close-loop time constant, \( \frac{1}{\beta \omega_{\text{unity}}} \) where \( \beta \) is the feedback factor.

The safe range for the \( \omega_4 \).

4. CMOS OP AMP circuit
**8-5.2 1V Rail-to-Rail CMOS OP AMPS**

1. Typical input stage for rail-to-rail amplifiers
   * Parallel-connected complementary differential pairs.
   * Operating zones for low VDD/VSS

2. Dynamic level-shifting current generator
   * The input resistance over the entire voltage range is infinite and no loading effect or input current over the previous stage.

   Usually mismatches cause negligible input current.
   * The symmetrical topology ensures very high CMRR

   \[ CMRR = \frac{1}{RG_m} \left( \frac{\Delta R}{R} + \frac{\Delta G_m}{G_m} \right)^{-1} \]

   where \( G_m = \Delta I / \Delta V_{i,cm} \)
3. Rail-to-rail very LV CMOS OP AMP with input dynamic level-shifting circuit

MAIN TRANSISTOR ASPECT RATIOS (IN \(\mu m\)) AND ELEMENT VALUES OF THE AMPLIFIER BASED ON COMPLEMENTARY PAIRS

<table>
<thead>
<tr>
<th>Transistor Pairs</th>
<th>Aspect Ratio</th>
<th>Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1A, M1B</td>
<td>400/5</td>
<td>M15</td>
<td>700/2</td>
</tr>
<tr>
<td>M2A, M2B</td>
<td>200/5</td>
<td>R1-R4</td>
<td>30 K(\Omega)</td>
</tr>
<tr>
<td>M1, M2</td>
<td>400/2</td>
<td>(R_M)</td>
<td>5 K(\Omega)</td>
</tr>
<tr>
<td>M3, M4</td>
<td>200/2</td>
<td>(C_M)</td>
<td>10pF</td>
</tr>
<tr>
<td>M5-M8</td>
<td>400/5</td>
<td>(I_{in} = I_{bp})</td>
<td>10(\mu A)</td>
</tr>
<tr>
<td>M9-M12</td>
<td>500/5</td>
<td>(I_o)</td>
<td>40(\mu A)</td>
</tr>
</tbody>
</table>

CHUNG-YU WU
4. Input CM adapter

\[ V_x = A[2V_{ref} - (V_{i+p} + V_{i-p})] \]
\[ = 2A(V_{ref} - V_{i,cm}) \]
\[ I = G_m V_x \]
\[ \Rightarrow V_{i,pcm} = V_{ref} + \frac{V_{icm}}{2RG_mA} \]
\[ V_{i,pm} = V_{i,dm} \]

*\( V_{i,cm} \) is degraded by A and \( V_{i,pcm} = V_{ref} \)

Circuit implementation:

5. Very LV CMOS OP AMP with a single differential pair and the input CM adapter.
Main transistor ratios (in µm) and element values of the amplifier based on a single input pair

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Ratio</th>
<th>Element Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1A-M1B</td>
<td>1000/6</td>
<td>M6: 1600/2</td>
</tr>
<tr>
<td>M2A-M2B</td>
<td>600/4</td>
<td>M7-M10: 300/4</td>
</tr>
<tr>
<td>MA1-MA4</td>
<td>50/2</td>
<td>M11: 700/2</td>
</tr>
<tr>
<td>MA5-MA6</td>
<td>300/4</td>
<td>R1-R2: 15KΩ</td>
</tr>
<tr>
<td>M2D</td>
<td>150/2</td>
<td>R_M: 5KΩ</td>
</tr>
<tr>
<td>M1,M2</td>
<td>200/2</td>
<td>C_M: 5pF</td>
</tr>
<tr>
<td>M3-M5</td>
<td>400/2</td>
<td>I_S=I_r/2: 10µA</td>
</tr>
</tbody>
</table>

6. Measured results

Experimental performance of amplifiers (V_supply=1V, technology: 1.2µm CMOS, C_L=15pF)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Dynamic-shifting amp</th>
<th>CM adapter amp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active die area</td>
<td>0.81mm²</td>
<td>0.26 mm²</td>
</tr>
<tr>
<td>I_do (supply current)</td>
<td>410µA</td>
<td>208µA</td>
</tr>
<tr>
<td>DC gain</td>
<td>87dB</td>
<td>70.5dB</td>
</tr>
<tr>
<td>Unity-gain frequency</td>
<td>1.9Mhz</td>
<td>2.1Mhz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>61°</td>
<td>73°</td>
</tr>
<tr>
<td>SR+</td>
<td>0.8V/µs</td>
<td>0.9V/µs</td>
</tr>
<tr>
<td>SR-</td>
<td>1V/µs</td>
<td>1.7V/µs</td>
</tr>
<tr>
<td>THD(0.5Vpp@1kHz)</td>
<td>-54dB</td>
<td>-77dB</td>
</tr>
<tr>
<td>THD(0.5Vpp@40kHz)</td>
<td>-32dB</td>
<td>-57dB</td>
</tr>
<tr>
<td>Vni(@ 1kHz)</td>
<td>267nV/√Hz</td>
<td>359nV/√Hz</td>
</tr>
<tr>
<td>Vni(@ 10kHz)</td>
<td>91nV/√Hz</td>
<td>171nV/√Hz</td>
</tr>
<tr>
<td>Vni(@ 1MHz)</td>
<td>74nV/√Hz</td>
<td>82nV/√Hz</td>
</tr>
<tr>
<td>CMRR</td>
<td>62dB</td>
<td>58dB</td>
</tr>
<tr>
<td>PSRR+</td>
<td>-54.4dB</td>
<td>-56.7dB</td>
</tr>
<tr>
<td>PSRR-</td>
<td>-52.1dB</td>
<td>-51.5dB</td>
</tr>
</tbody>
</table>

§8-5.3 1.5V High Drive Capability CMOS OP AMP

1. Folded-mirror differential input stage

\[ V_{CM} \leq V_{GS_{6,7}} + V_{THn} = 2V_{THn} + \Delta V_{6,7} \]

\[ V_{CM} \geq V_{DS_{Sat}} + V_{GS_{1,2}} = 2V_{THn} + \Delta V_{5} + \Delta V_{1,2} \]

\[ CMR = V_{THn} - \Delta V_{5} \]

\( \Delta V \) : overdrive voltage.

CMR is independent of supply voltage.

For \( V_{DD} = 1.5V \), CMR = 0.6 ~ 0.7V

CMR of the conventional NMOS-input differential pair is 0.3-0.5V

2. Output Stage

Input section: M1A-M4A , \( I_{B1} \), \( I_{B2} \)

Output section: M5A-M6A and M7A-M8A

M5A, M8A sat

M6A, M7A off.

For low input levels, M6A and M7A off \( \Rightarrow \) Class A operation.

For large positive input signals,

\( I_{D1A} = I_{B1} \Rightarrow M3A \) and M5A OFF

\( \Rightarrow V_A \uparrow -V_{SS} \)

\( \Rightarrow M_{6A} \) is turned on to supply most of the output current.

But M7A remains cutoff.

The current of M8A is increased.

For large negative input signals, M7A supplies most of the output current.

\( (W/L)_{5A,8A} \ll (W/L)_{6A,7A} \) for low dc power dissipation and high drive.
3. Overall LV CMOS OP AMP.

Dominant pole: \( W_{p1} \approx \frac{1}{r_{o5,7} \{ (g_{m8} r_{o8,9})2 [g_{m5A,8A} (r_{o5A} \| r_{o8A})] \} C_c} \)

Gain-bandwidth product: \( W_{GBW} \approx \frac{g_{m1,2}}{C_{c1}} \)

Hybrid nested Miller compensation: \( C_{C1}, C_{C2}, C_{C3A,B} \)

The inner amplifier \( M_8, M_9, M_{1A} \sim M_{8A} \) contributes the nondominant poles.

* The two-stage OP AMP \( M_1 \sim M_9 \) has a gain-bandwidth product of \( \frac{g_{m1,2}}{C_{c2}} \) and the gain of \( \frac{g_{mIII}}{sC_{c1}} \) at high frequency. The gain of \( M_1 \sim M_7 \) at high frequency is \( \frac{g_{mIII}}{sC_{c1}} \). Thus the gain of the gain stage \( M_8 \) and \( M_9 \) is approximately equal to \( \frac{C_{C1}}{C_{C2}} \).

* The open-loop gain of the inner amplifier is

\[
A_m = \left( \frac{C_{C1}}{C_{c2}} \right) \frac{g_{m1A,2A}}{g_{m3A,4A}} 2 g_{m5A,8A} (r_{o5A} \| r_{o8A})
\]

Dominant pole: \( \omega_{p1m} = \frac{g_{m3A,4A}}{g_{m5A,8A} (r_{o5A} \| r_{o8A}) C_{C3A,B}} \)

Second pole: \( \omega_{p2m} = \frac{2 g_{m5A,8A}}{C_L} \)
Gain-bandwidth product: \( \omega_{GBWin} = 2 \frac{g_{m1A,2A}}{C_{C2}} \frac{C_{C3A,B}}{C_{C1}} \)

or the second pole of the whole amplifier

Design consideration:

To obtain a maximally flat Butterworth response without gain peaking, we have the unity-gain frequency equal to one half of the second-pole frequency.

\[
\omega_{GBWin} = \omega_{uin} = \frac{1}{2} \omega_{P2in}
\]

\[
\omega_{GBW} = \omega_a = \frac{1}{2} \omega_{uin} = \frac{1}{2} \omega_{GBWin}
\]


Setting \( 2C_{C3A,B} = C_{C2} \), we have

\[
C_{C1} = 2 \frac{g_{m1,2}}{g_{m5A,8A}} C_L
\]

\[
C_{C2} = 2C_{C3A,B} = \sqrt{2} \frac{g_{m1,2} g_{m1A,2A}}{g_{m5A,8A}} \cdot \frac{C_L}{C_{C3A,B}}
\]

Component values:

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M9, M1A, M2A, M10</td>
<td>60/2</td>
</tr>
<tr>
<td>M4, M5, M11, M12, M13</td>
<td>20/2</td>
</tr>
<tr>
<td>M6, M7</td>
<td>15/2</td>
</tr>
<tr>
<td>M8</td>
<td>90/2</td>
</tr>
<tr>
<td>M3A</td>
<td>5/1.2</td>
</tr>
<tr>
<td>M4A</td>
<td>15/1.2</td>
</tr>
<tr>
<td>M5A</td>
<td>30/1.2</td>
</tr>
<tr>
<td>M7A</td>
<td>120/1.2</td>
</tr>
<tr>
<td>M6A</td>
<td>360/1.2</td>
</tr>
<tr>
<td>M8A</td>
<td>90/1.2</td>
</tr>
<tr>
<td>M14, M16</td>
<td>10/1.2</td>
</tr>
<tr>
<td>M15, MC</td>
<td>30/2</td>
</tr>
<tr>
<td>C\text{C}_1</td>
<td>4pF</td>
</tr>
<tr>
<td>C\text{C}_2</td>
<td>6pF</td>
</tr>
<tr>
<td>C\text{C}<em>{3A}, C\text{C}</em>{3B}</td>
<td>2pF</td>
</tr>
<tr>
<td>I_{BIAS}</td>
<td>5uA</td>
</tr>
<tr>
<td>V_{TH}</td>
<td>0.8V</td>
</tr>
</tbody>
</table>
Experimental results:

**MEASURED MAIN PERFORMANCE**

<table>
<thead>
<tr>
<th>Performance Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open-Loop Gain</td>
<td>68dB</td>
</tr>
<tr>
<td>GBW</td>
<td>1MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>65°</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>16dB</td>
</tr>
<tr>
<td>Settling Time (0.1%)</td>
<td>400ns</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>1 V/μs</td>
</tr>
<tr>
<td>THD@1kHz V_{out} = 0.5V</td>
<td>-57dB</td>
</tr>
<tr>
<td>Closed-Loop Gain</td>
<td>20dB</td>
</tr>
<tr>
<td>PSRR+@1kHz</td>
<td>75dB</td>
</tr>
<tr>
<td>PSRR-@1kHz</td>
<td>75dB</td>
</tr>
<tr>
<td>CMRR@1kHz</td>
<td>95dB</td>
</tr>
<tr>
<td>Offset</td>
<td>&lt; 8mV</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>280 μW</td>
</tr>
<tr>
<td>Die Size</td>
<td>0.08 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>1.2 μm CMOS</td>
</tr>
<tr>
<td>Loading</td>
<td>50pF</td>
</tr>
</tbody>
</table>
Chapter 9 Passive Components and Switches

§ 9-1 Resistors

1. Source/Drain diffused resistor

* Compatible with NMOS and CMOS, metal-gate and Si-gate technologies.
* $R_\square = 20 \sim 100\Omega / \square \ (100K\Omega \ max)$
* Temperature Coefficient of Resistance (TCR) = 500~1500 ppm/°C
  Voltage Coefficient of Resistance (VCR)=100~500ppm/°C
  Tolerance=±20% (Absolute)
* High parasitic capacitance (n$^+$-p junction cap.)
  Piezoresistance error. (Because of shallow junction)

2. P-well (N-well) diffused resistor (Well or tub resistor)

* Compatible with CMOS metal-gate or Si-gate technology.
* $R_\square = 1K\Omega \sim 5K\Omega / \square$
  Large VCR
Tolerance=±40% (absolute)

* Large depth and lateral spreading ⇒ narrow resistors are impossible.

3. Implanted resistor

![Implanted Resistor Diagram]

* Compatible with NMOS and CMOS, metal-gate and Si-gate technologies.
* Need an additional masking step.
* \( R_{\text{in}} > 500\Omega \sim 1000\Omega / \square \); can be accurately controlled.
* Higher VCR; smaller tolerance.
* Difficult to eliminate the piezoresistance effect.
* The resistor implant can be combined with the depletion implant.

4. Poly-Si resistor

![Poly-Si Resistor Diagram]

* Realizable by NMOS and CMOS Si-gate technologies.
* \( R_{\text{in}} = 30\Omega \sim 200\Omega / \square \) (doped with the source/drain diffusion)
* TCR\( \approx \) 500~1500 ppm/°C; Tolerance=±40%
* Can be trimmed by laser or poly fuse.
* Fully isolated with smaller parasitic capacitance.
  ◊ Version I: Poly-I resistor
  ◊ Version II: Poly-II resistor
  ◊◊ Version III: Poly-I and Poly-II distributed RC structure
    (please see the structure shown in poly to poly capacitor)

5. Switched-capacitor simulated resistor
   * Realizable by NMOS and CMOS, metal-gate and Sigate technologies.
   * High frequency operation?

\[
i = \frac{V_1 - V_2}{R}
\]

\[
f_c \text{ is the clock frequency of } \phi \text{ or } \bar{\phi}
\]

\[
i = \frac{C(V_1 - V_2)}{T}, \quad R = \frac{T}{C} = \frac{1}{f_c \cdot C}
\]

6. Thin-film resistor
   * Realizable by NMOS and CMOS, metal-gate and Si-gate technologies.
   * Need additional process steps.
   * Si-Chromium resistor or Mo resistor.
   * Laser trimming is possible.
   * Non-conventional material may be involved.

§ 9-2 Capacitors
1. PN junction capacitor
   * Well known and understood.
   * Nonlinear capacitance with a large VCR.
* Compatible with all MOS technologies.

2. MOS capacitor

![MOS capacitor diagram]

* Realizable only by NMOS and CMOS metal-gate technology.
* TC=25 ppm/°C
  Tolerance=±15%
  VC=25ppm/V
* Voltage-dependent capacitance
  accumulation depletion
  $C_o = (C_o^{-1} C_d^{-1})^{-1}$

3. Poly (or metal ) to bulk silicon capacitor

![Poly (or metal ) to bulk silicon capacitor diagram]

* Realizable by NMOS and CMOS poly-Si-gate (metal-gate ) technologies.
* Need an extra mask to define the heavy $n^+$ implant as the bottom plate.
* Can be trimmed by laser on poly-fuse.
  ( Poly-fuse : blown with 10-20mA )
* Bottom plate pn junction parasitic capacitance ($\approx 15\% - 30\%$)
* VC of the capacitor$\approx -10$ppm/V
* TC $\approx$ 20-50 ppm/$^\circ$C
* Tolerance = $\pm$15%

4. Poly to field implant region capacitor

![Diagram of poly to field implant region capacitor]

* Realizable only by NMOS and CMOS Si-gate technologies with the field implant.
* Smaller oxide capacitance per unit area
  - Thick field oxide
* The capacitor’s bottom plate must be always connected to the substrate.
* Low quality dielectric oxide.

5. Metal to poly capacitor

![Diagram of metal to poly capacitor]

* Realizable by NMOS and CMOS Si-gate technologies.
* Interdielectric is poly-oxide.
* Extra mask to define the poly-oxide pattern.
* Poly fuse trimming is possible.
* CVD oxide is not good as capacitor dielectric
hysteresis in Q-V due to dielectric changing and relaxation.

* For reliability consideration, the top metal layer must be larger than the poly oxide layer.
  ⇒ $C_{\text{Thick}}$ exists
  ⇒ parasitic capacitance
* $VC=100\text{ppm/v}$, $TC=100\text{ppm/}^\circ\text{C}$

6. poly to poly capacitor

* Realizable by NMOS and CMOS double-poly technologies.
* $VC=100\text{ppm/v}$
  $TC=100\text{ppm/}^\circ\text{C}$
* Double-poly
  ⇒ EPROM or $E^2\text{PROM}$ are available
  ⇒ may be applied in trimming
* The poly2 area may be smaller than the poly-oxide area
  ⇒ small $C_{\text{Thick}}$


§ 9-3 Tolerance Considerations.
Resistors: Absolute tolerance $\approx \pm 20\% \sim \pm 40\%$
  Matching or ratio tolerance $\approx \pm 0.1\% \sim \pm 10\%$
Capacitors: Absolute tolerance $\approx \pm 15\%$
Matching or ratio tolerance \( \approx \pm 0.01\% \sim \pm 1\% \)

 Resistors:

\[
R = \frac{R_s}{W} \frac{L}{W}, \quad \frac{\Delta R}{R} = \frac{\Delta L}{L} - \frac{\Delta R_s}{R_s} \approx \frac{\Delta L}{L} - \frac{\Delta W}{W}
\]

If \( L \) is large \( \Rightarrow \frac{\Delta L}{L} \approx 0 \Rightarrow \frac{\Delta R}{R} \approx \frac{\Delta W}{W} \)

\[
R = \frac{\rho}{X_t} \frac{L}{W}, \quad \sigma_R = \left[ \left( \frac{\delta \rho}{\rho} \right)^2 + \left( \frac{\delta L}{L} \right)^2 + \left( \frac{\delta W}{W} \right)^2 + \left( \frac{\delta X_t}{X_t} \right)^2 \right]^{1/2}
\]

\[
= \frac{\delta W}{W} \quad \text{for long resistor}
\]

* Long resistor pattern is recommended in precise resistors.

 Capacitors:

\[
C = \frac{\varepsilon_{sio2}}{t_{ox}} WL, \quad \frac{\Delta C}{C} = \frac{\Delta W}{W} + \frac{\Delta L}{L} + \frac{\Delta \varepsilon_{sio2}}{\varepsilon_{sio2}} - \frac{\Delta t_{ox}}{t_{ox}}
\]

 edge effect Oxide effect

 CASE I: Absolute tolerance

\[
\frac{\Delta C}{C} = \frac{\Delta W}{W} + \frac{\Delta L}{L} \quad \text{(if W and L are small or } \Delta \varepsilon_{sio2} \text{ and } \Delta t_{ox} \text{ are negligible)}
\]

If \( \square \) W and \( \square \) L are independent with \( \sigma_{\Delta l} = \sigma_{\Delta w} = \sigma_l \)

\[
\sigma_{\Delta C} = \sigma_{l} \sqrt{\frac{L}{W^2} + \frac{L}{L^2}} \quad \text{(random variation)}
\]

Assume \( L=W=d \), \( \sigma_{\Delta C} = \frac{\sqrt{2 \sqrt{l}}}{d} \) is minimum

\[
\Rightarrow \sigma_{\Delta C} \mid \text{square} (L=W) < \sigma_{\Delta C} \mid \text{non-square} (W \neq L)
\]

For the same WL , minimum perimeter leads to minimum tolerance.

 Circular shape?

 CASE II: Ratio or Matching tolerance under geometry random variation
\[ \alpha = \frac{C_1}{C_2} = \frac{W_1L_1}{W_2L_2} , \quad \frac{d\alpha}{\alpha} = \frac{dC_1}{C_1} - \frac{dC_2}{C_2} \]

\[ \sigma_{d\alpha} = \frac{\sigma_{dc_1}}{\sqrt{\frac{\sigma_{dc_1}^2 + \sigma_{dc_2}^2}{c_1}}} = \sigma_l \sqrt{\frac{I}{L_1^2} + \frac{I}{W_1^2} + \frac{I}{L_2^2} + \frac{I}{W_2^2}} \]

For \( W_2=L_2=d \), \( \sigma_{d\alpha} = \frac{\sigma_l}{d} \sqrt{2 + \frac{L_1^2 + W_j^2}{(\alpha d)^2}} \)

\[ \Rightarrow \frac{\sigma_{d\alpha}}{\alpha_{min}} = 2 \frac{\sigma_l}{d} \quad \text{if} \quad L_j = W_j = \sqrt{\alpha}d \quad (1) \]

square versus square

CASE III : Ratio tolerance under the uniform undercut effect

Uniform undercut is not a random variation.

\[ \alpha = \frac{C_1}{C_2} = \frac{W_1L_1}{d^2} \]

\[ \alpha_{actual} = \frac{W_1L_1 - P_j\Delta x + 4\Delta x^2}{d^2 - P_j\Delta x + 4\Delta x^2} \approx \frac{W_1L_1 - P_j\Delta x}{d^2 - P_j\Delta x} \]

\[ \frac{\Delta\alpha}{\alpha} \approx \frac{\Delta x}{d^2}(P_2 - \frac{P_1}{\alpha}) \]

IF \( P_2 = \frac{P_1}{\alpha} \Rightarrow \Delta\alpha \equiv 0 \quad \text{i.e.} \quad 4d = \frac{2(W_j + L_j)}{\alpha} \]

So

\[ \begin{cases} W_1L_1 = \alpha d^2 \\ 2(W_1 + L_j) = 4d\alpha \end{cases} \]

\[ \Rightarrow W_j = d(\alpha - \sqrt{\alpha^2 - \alpha}) ; \quad L_j = d(\alpha + \sqrt{\alpha^2 - \alpha}) \quad (2) \]

\[ \sigma_{d\alpha} = \frac{\sigma_l}{d} \sqrt{6 - \frac{2}{\alpha}} \approx \frac{\sigma_l}{d} \sqrt{6} \]

If \( \alpha = l \), both conditions (1) and (2) can be satisfied

\[ \Rightarrow \text{Ratio tolerance} \downarrow \]
CASE IV: Ratio tolerance under edge and oxide effects

Take $\alpha = 1 \Rightarrow$ unit capacitor array

\[ \frac{C_1}{C_2} \]

- Centralized structure to avoid the oxide effect.
- Dummy capacitor may be omitted to save area.
- Ratio tolerance can be $\pm 0.06\%$

Similarly, for resistors, we have

\[ R_1 \quad R_2 \quad R_1 \quad R_2 \]

- Ratio tolerance can be $\pm 0.25\%$

§ 9-4 The MOS Switch

1. The NMOS switch

   1) If $V_{\phi} \geq V_1 + V_{THN}$, $M_N$ on $\Rightarrow V_2 = V_1$ full transmission
Example:
$V_1 = 0 \text{V}, \ V_\phi = 3 \text{V} \Rightarrow V_2 = 0$
$V_1 = 5 \text{V}, \ V_\phi = 8 \text{V}, \ V_{TN} = 1.5 \text{V} \Rightarrow V_2 = 5 \text{V}$

2) If $V_1 + V_{THN} > V_\phi > V_{THN}, \ M_N \text{ on}$

$V_2 = V_\phi - V_{THN}$

Example: $V_\phi = 5 \text{V}, \ V_1 = 5 \text{V}, \ V_{THN} = 1.5 \text{V}$ (under substrate bias), $V_{BS} = 0 \text{V}$

$\Rightarrow V_2 = 3.5 \text{V}$

3) If $V_\phi < V_{THN}, \ M_N \text{ off}$

Node 1 or 2 may be floating

$\Rightarrow V_1 \text{ or } V_2 \text{ will be gradually charged or discharged by the leakage current in } \text{MOS or PN junctions.}$

If $V_\phi = 0 \text{V}$ for a very long time, $V_A \rightarrow 0 \text{V}$ by the $n^+p$ junction leakage current $\Rightarrow$ Not allowable in circuit design

* When the switch is turned on or off, the charging or discharging current is nonlinear $\Rightarrow$ Nonlinear resistor

Capacitance feedthrough effect:
\[ V_0 : V_{DD} \to 0 \]

\[ V_{1f} \approx V_{1i} - V_{DD} \frac{C_{gs}}{C_{gs} + C_1} \]

\[ V_{2f} \approx V_{2i} - V_{DD} \frac{C_{gd}}{C_{gd} + C_1} \]

error voltage

Example: \( C_{gd} \approx 0.02\,\text{PF}, C_2 = 2\,\text{PF}, V_{DD} = 10\,\text{V} \), error voltage \( \approx 0.1\,\text{V} \)

Compensation circuit:

2. The PMOS switch

* Can pass high voltage without offset.

Example: \( V_0 = 0\,\text{V} \), \( V_{DD} = 5\,\text{V} = V_i \)

\[ \Rightarrow V_2 = 5\,\text{V} \quad \therefore \text{I = source} \quad \text{and} \quad |V_{GS}| = 5\,\text{V} \]
* Can’t pass low voltage completely.

Example: $V_0 = 0V$, $V_{2i} = 5V$, $V_I = 0V$, $|V_{TP}| = 1.5V$

$\Rightarrow V_{2f} \approx 1.5V \neq 0V$

3. The CMOS switch

* Full transmission
* The clock feedthrough effect can be greatly compensated, if the delay between $V_\phi$ and $V_\phi$ is zero.
* Nonlinear $C_{gs}$ and $C_{gd}$ and the delay between $V_\phi$ and $V_\phi$ make the compensation of the feedthrough effect quite complicated.
* If $V_I = 5V = V_\phi, V_\phi = 0V, V_{DD} = 5V, V_{TN} = |V_{TP}| = 1.5V$

$V_2 = 0V \rightarrow V_2 = 5V - 1.5V = 3.5V$ : NMOS and PMOS

$V_2 = 3.5V \rightarrow V_2 = 5V$ : Only PMOS

If $V_I = 0V, V_{2i} = 5V$

$V_2 = 5V \rightarrow V_2 = 1.5V$ : NMOS and PMOS

$V_2 = 1.5V \rightarrow V_2 = 0V$ : Only NMOS
§10-1 Basic Principles of Bandgap References (BGR)

\[ V_{BE(on)} = mV_{therm} \ln(I_1 / I_S) \]

\[ I_S = qA n_i \bar{D}_n / Q_B \]

\[ I_S : \text{Reverse saturation current of a BJT} \]

\[ = B n_i \bar{D} \]

\[ A : \text{Area of a BJT} \]

\[ = B n_i^2 T \bar{\mu} \]

\[ Q_B : \text{Base minority carrier charges} \]

where \( B \) and \( \bar{B} \) are constants, indep. of T.

\[ \bar{\mu} = C T^{-n} \]

\( C \): Constant, indep. of T.

\( n \): Temp. exponent.

\[ n_i^2 = ET^3 \exp(-V_{GO}/V_{therm}) \]

\( E \): Constant, indep. of T.

\( V_{GO} \): Energy gap.

\[ \Rightarrow V_{BE(on)} = mV_{therm} \ln[I_1 T^{-\gamma} F \exp(V_{GO}/V_{therm})] \]

\( F \): Constant, indep. of T.

\( \gamma = 4 - n \)

\[ I_1 = GT^\alpha \]

where \( I_1 \) is the collector current and \( G \) is a temp.-indep. constant.

\[ \Rightarrow V_{BE(on)} = V_{GO} - mV_{therm} (\gamma - \alpha) \ln T - \ln(FG) ] \]

In general, the output voltage \( V_{out} \) is a sum of \( V_{BE(on)} \), and \( KV_{therm} \) with a weighting factor K such that \( V_{out} \) is nearly indep. of T.

\[ V_{BE(on)} + KV_{therm} = V_{out} = V_{GO} - mV_{therm} (\gamma - \alpha) \ln T + mV_{therm} [K + \ln(FG)] \] .......(1)

\[ \frac{dV_{out}}{dT} \bigg|_{T = T_o} = 0 = \frac{mV_{therm}}{T_o} [K + \ln(FG)] - \frac{mV_{therm}}{T_o} (\gamma - \alpha) \ln T_o - \frac{mV_{therm}}{T_o} (\gamma - \alpha) + \frac{d}{dT} V_{GO} \]

\[ \Rightarrow K + \ln(FG) = (\gamma - \alpha) \ln T_o + (\gamma - \alpha) - \left( \frac{d}{dT} V_{GO} \right) \cdot \frac{T_o}{mV_{therm}} \] .......(2)

Substituting (2) into (1), we have
$$V_{out} = V_{GO} + mV_{\text{therm}}(\gamma - \alpha)(1 + \ln \frac{T_o}{T}) - T \frac{d}{dT} V_{GO}$$

$$V_{GO} = 1.16 - \frac{7.02 \times 10^{-4} \cdot T^2}{T + 1108}$$

$$\frac{d}{dT} V_{GO} \bigg|_{T=T_o} = - \frac{14.04 \times 10^{-4} T_o (T_o + 1108) - 7.02 \times 10^{-4} \cdot T_o^2}{(T_o + 1108)^2}$$

$$= - \frac{14.04 \times 10^{-4} \cdot T_o + 7.02 \times 10^{-4} \cdot T_o^2}{T_o + 1108} \frac{T}{(T_o + 1108)^2}$$

$$\Rightarrow V_{out} = mV_{\text{therm}}(\gamma - \alpha)(1 + \ln \frac{T_o}{T}) + 1.16 - \frac{7.02 \times 10^{-4} \cdot T^2}{T + 1108} - \frac{14.04 \times 10^{-4} \cdot T_o T}{T_o + 1108} + \frac{7.02 \times 10^{-4} \cdot T_o^2 \cdot T}{(T_o + 1108)^2}$$

If $\gamma = 3.2, m = 1, \alpha = 1, T_o = 25^\circ C$

$$\Rightarrow V_{out}(T) \big|_{T=25^\circ C} = 1.16 + 2.2(0.0259) - \frac{21.06 \times 10^{-4}(298)^2}{298 + 1108} + \frac{7.02 \times 10^{-4}(298)^2}{(298 + 1108)^2}$$

$$= 1.093 V$$

§10-2 Bipolar Bandgap Reference

Widlar bandgap reference

* Feedback element $Q_4$ is used to force $Q_3$ on.

* $Q_4$ also serves as a start-up circuit.

* $V_{out} = I_2 R_2 + V_{BE3}$

$I_2 = I_3$ if $I_{B2} = I_{B3}$

$\frac{I_3}{R_3} = \frac{V_{BE1} - V_{BE2}}{R_3} = \frac{1}{R_3} m V_{\text{therm}} \left[ \ln \frac{I_2}{I_3} + \ln \frac{I_{S2}}{I_{S1}} \right]$

$V_{out} = V_{BE3} + \left[ \frac{R_2}{R_3} m \left[ \ln \left( \frac{R_2}{R_1} \right) + \ln \left( \frac{I_{S2}}{I_{S1}} \right) \right] \right] \cdot V_{therm}$

$I_1 / I_2 = R_2 / R_1$ if $V_{BE1} = V_{BE3}$

Adjust $R_2 / R_3$, $R_2 / R_1$ and $I_{S2} / I_{S1}$ to give a suitable $K$

And Keep $I \equiv I_2$ to obtain $I_{B2} \equiv I_{B3}$ and $\frac{I_{S3}}{I_{S1}} = \frac{I_3}{I_1}$ to obtain $V_{BE1} = V_{BE3}$.
§10-3 CMOS Real Bandgap Reference (BGR)

§10-3.1 CMOS BGR via BJTs and Resistors

Version 1:
N-well CMOS, positive $V_{\text{REF}}$

Version 2:
N-well CMOS, Negative $V_{\text{REF}}$

Q1, Q2: Substrate-well-source/drain parasitic vertical BJTs

$V_{BE} = mV_{\text{therm}} \ln \frac{I_E}{I_S}$

$V_{\text{REF}} = \pm [V_{BE1} + \frac{R_2}{R_3} V_{\text{therm}} (\ln \frac{R_2}{R_1} + \ln I_{Q2}) + V_{OS} \frac{R_3 + R_2}{R_3}]$

The operating point ④ is the desired operating point => Need a start-up circuit.
Typical design values:

\[ I_1 = 80 \mu A \quad I_2 = 8 \mu A \]

\[ R_2 \approx \frac{0.6 V}{8 \Omega} = 75 K \Omega, \quad R_1 = \frac{R_2}{10} = 7.5 K \Omega, \quad R_3 = \frac{60 mV}{8 \Omega} = 7.5 K \Omega \]

Large resistance \( \Rightarrow \) use well resistors

R1, R2, R3: n+/p+ diffusion resistors
n+ - poly resistors
well resistors

Both transistors are in the active region

Error analysis:

1. Error due to base resistances

\[ V_{BE1} = V_{therm} \ln \frac{I_1}{I_S} + V_{therm} \ln \frac{1}{1 + \frac{1}{I_1 R_1}} + \frac{r_b I_1}{A \Phi_1} \]

\[ \Delta V_{BE} = V_{therm} \ln A + V_{therm} \ln \frac{I_2}{I_1} + V_{therm} \ln \frac{1}{1 + \frac{1}{I_2 R_2}} + \frac{r_b (I_2 - I_1)}{A \Phi_2} \]

If \( \hat{a}_1, \hat{a}_2 \) are not large enough or \( r_b \) is too large,

\[ \Rightarrow \Delta V_{BE} \text{ due to } r_b \text{ and } \Phi \text{ is large.} \]

\[ V_{REF} = \pm \left[ V_{BE1} + V_{OS} \left( \frac{R_3 + R_2}{R_3} \right) + \frac{R_2 V_{therm}}{R_3} \left( \ln \frac{R_2}{R_1} + \ln \frac{I_2}{I_s} + \ln \frac{1}{1 + \frac{1}{I_2 R_2}} + \frac{R_2}{R_3} \left( \frac{I_2}{A \Phi_2} - \frac{I_1}{A \Phi_1} \right) \right) \right] \]

2. Error due to input offset voltage \( V_{os} \)

\[ V_{os} = 10 mV, \quad V_{os} (1 + \frac{R_2}{R_3}) \approx 10 V_{os} = 100 mV \]

TC error due to

\[ V_{os} \cdot \frac{1}{V_{REF}} \frac{d}{dT} V_{REF} = \frac{(1 + \frac{R_2}{R_3}) V_{os}}{V_{REF} T_0} = \frac{10 \times 10 mV}{1.26 V \times 300 K} = 264 \text{ ppm } / ^\circ C \]

3. Error due to Bias current variation

\[ V_{BE1} = V_{therm} \ln \frac{I_1}{I_s} = V_{therm} \ln \frac{\frac{V_{therm}}{R}}{I_s} \]

(R3=R1)
\[ V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O)I_{S1}} + V_{therm} \ln \frac{R_1(T_O)}{R_1(T)} \quad I_1 = I_2 \]

If \( R_1 \) is indep. of \( T \) \( \Rightarrow V_{BE} = V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O)I_{S1}} \)

If \( R_1 \) depends on \( T \) \( \Rightarrow V_{BE} = V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O)I_{S1}} + V_{therm} \ln \frac{R_1(T_O)}{R_1(T)} \)

\[ V_{BE} = V_{BE|ideal} - V_{therm} \left( \frac{1}{R} \frac{dT}{dT_{ref}} \right) (T - T_O) - V_{therm} \left( \frac{1}{2R} \frac{dT^2}{dT_{ref}} \right) (T - T_O)^2 + V_{therm} \left( \frac{1}{2R^2} \frac{dT^3}{dT_{ref}} \right) (T - T_O)^3 - \ldots \]

If \( R \) is only linearly dependent on \( T \), we still have \( PTAT^2 \) term
The \( PTAT^2 \) term can be cancelled via curvature compensations.

4. TC Error due to Base Resistance

\[ \Delta V_{BE} = r_b \frac{I_2}{\beta_2} \]

\[ \text{TC error} = \left( 1 + \frac{R_2}{R_1} \right) \frac{r_b I_2}{V_{ref} \beta_2} \left( \frac{1}{r_b} \frac{dr_b}{dT} + \frac{1}{I_2} \frac{dI_2}{dT} - \frac{1}{\beta_2} \frac{d\beta_2}{dT} \right) \]

Example: \( r_b = 2K\Omega \), TC of \( r_b = 1000 \text{ppm} / ^\circ C \), \( I_2 = 30\mu A \), \( \beta = 150 \),

TC of \( \beta = 7000 \text{ppm} / ^\circ C \)

\( \Rightarrow \) TC = –8.6 \text{ ppm} / ^\circ C

5. Error due to base current

Base current cancellation technique

*To compensate for the difference between the collector, emitter, or base current

The circuit to obtain $V_{REF}$ from a BGR

1. $V_{O} = V_{BE1} + V_{BE2} + V_{BE3} \cdot \frac{K}{T} \ln(\alpha)$
   *Better matching

2. $V_{O} = V_{BE3} + \frac{K}{T} \ln(\alpha \cdot \gamma) \cdot (1 + R/R) \Rightarrow$ Bandgap Reference
5. Low Power Supply Circuit:

*Low driving capability

Power supply limits:

<table>
<thead>
<tr>
<th>Bandgap reference</th>
<th>Low Possible</th>
<th>Voltage</th>
<th>T=25°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>PMOS Inputs</td>
<td>NMOS Inputs</td>
<td></td>
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<tr>
<td></td>
<td>V_{TP} ≤ 1.0V</td>
<td>V_{TN} ≤ 1.0V</td>
<td></td>
</tr>
<tr>
<td>1</td>
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<td></td>
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<tr>
<td>2</td>
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<td>2.95v</td>
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</tr>
<tr>
<td>3</td>
<td>1.90v</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>2.5v</td>
<td>1.5v</td>
<td></td>
</tr>
</tbody>
</table>

> **10-3.3 CMOS BGR via lateral Transistor**


Structure of a lateral BJT in CMOS:
Voltage reference via LBJT:
Conceptual circuit:

Advantages:
(1) The offset of the amplifier A has a negligible effect on $V_{REF}$.
(2) Simple structure.

Purpose of VCC: To provide a current path for $I_{R1} >> I_{B1}, I_{B2}$
* High supply voltage.
* Two source followers + one emitter follower
  $\text{in}(A) \text{ current amp.} \Rightarrow \text{higher current gain}
* Low supply voltage
* Low current gain in A
* R2 is trimmable

R4, R3, T3: VCC

R3: To keep T3 from quasi-saturation
R4: To sense the output voltage and transform it into the collector current of T3.

* All resistor are polyresistors
* Low output impedance.

Measured results:

- $V_{\text{REF}}$ mean: 1.2285V; standard deviation: 150µV
- Minimal supply voltage: 2.2V
- Supply current: 79µA
- Noise spectra: $316nV/\sqrt{\text{Hz}}$ (white); $560nV/\sqrt{\text{Hz}} (1kHz)$
- PSRR(100Hz): 60dB
- Load regulation ($\Delta V_{\text{out}}/I_{\text{out}}$): 3.6µV/µA
- Chip area: 0.42 mm²
High PSRR BGR:
* $R_1, R_2$ may be p-well resistors and PSRR still high.

Experimental results:
- $V_{REF} = 1.2281 \text{V (mean)}$
- $350 \text{mV (} \sigma \text{)}$
- Minimal Supply = 1.7V
- Supply Current = 20\text{mA}
- Noise Spectra: $500nV/\sqrt{\text{Hz}}$ (white)
- $1\mu V/\sqrt{\text{Hz}}(1KHz)$
- PSRR (100Hz) = 77dB
- Load Regulation: $4.1mv/\mu A$
- Chip area = $0.18 \text{mm}^2$

Curvature-Compensated BGR:


§10-4 High-Precision Curvature-Compensated CMOS Bandgap Voltage References (BVR)


1. Type A structure

The circuit structure of the proposed BVR (Type A)
$$V_{\text{out}} = V_{BE3} + I_3 r_2 = V_{BE3} + r_3 \frac{R_3}{R_1} \left( \frac{kT}{q} \ln A^* + \Delta V_{sg} \right)$$

2. Type $\bar{A}$ structure

3. Type B structure
4. Type C structure

The cascode structure of BVR (Type C):

The variation of $\Delta V_{sg}$ versus temperature
The simulated output voltages versus temperature in Type A and Type A BVR

The variation of $\Delta V_{sg}$ versus MOS channel length in Type A BVR
The Spice simulated output voltages versus temperature in Type C BVR

![Graph showing Spice simulated output voltages versus temperature in Type C BVR.](image)

The measured output voltages versus temperature in the fabricated cascaded-structure BVR (Type C) [3.5 μm CMOS technology, $R_1=1\,\text{KΩ}\,\text{external}$, $R_2=25.9\,\text{KΩ}\,\text{external}$]

![Graph showing measured output voltages versus temperature in the fabricated cascaded-structure BVR (Type C).](image)
* Average temperature drift
  5.5 ppm/°C  -60 °C ~ +150 °C
  5V~15V
* At 25 °C, average voltage drift 25μV/V
  Vout=1.1963V  ~  1.1965V
  5V  ~  15V
* 2 mil², 0.8 mW at 5V

§10-5 CMOS Bandgap Reference with Sub-1-V Operation
Ref.: IEEE JSSC, vol.34, pp.670~674, May 1999

Concept: * Convertional BGR  \( V_{ref} = 1.25V \)

  Can’t be operated below 1V supply.

* The built-in voltage  \( V_f \) of the diode  \( \rightarrow \) the current  \( I_{2b} \)
  The thermal voltage  \( V_{therm} \)  \( \rightarrow \) the current  \( I_{2a} \)

  \( (I_{2a} + I_{2b})R \rightarrow V_{ref} < 1V \)

1. Schematic of the proposed BGR

[Diagram of the proposed BGR]

Native NMOS  \( V_{THI} = -0.2V \)
NMOS  \( V_{THN} = +0.7V \)
PMOS  \( V_{THP} = -1.0V \)
*The diode is realized by the parasitic $P^+/n$-well/$P$-substrate BJT as

![Diode symbol]

* $C_1$ and $C_2$ are used to stabilize the circuit.
* The control signal PONRST is used to initialize the BGR circuit when the power is turned on.
* $R_1 = R_2$
  $\frac{V_a}{V_b} = 3$
  $I_1 = I_2 = I_3$ and $I_{1a} = I_{2a}$, $I_{1b} = I_{2b}$
  $dV_f = V_{f1} - V_{f2} = V_{\text{therm}} \ln(N)$, $N = 100$

\[
I_{2a} = \frac{dV_f}{R_3} \propto V_{\text{therm}}
\]
\[
I_{2b} = \frac{V_{f1}}{R_2} \propto V_f
\]
\[
I_3 = I_2 = I_{2a} + I_{2b}
\]
\[
V_{\text{ref}} = R_1 I_3 = \frac{R_1}{R_2} V_{f1} + \frac{R_1}{R_3} dV_f
\]

2. Simulated $V_{\text{ref}}$ characteristics

![Graph showing simulated $V_{\text{ref}}$ characteristics]
$V_{ref} = 1.25V$  conventional BGR

$V_{ref} = 0.84V$  proposed BGR

3. Minimum $V_{DD}$

$$
\min V_1 \equiv V_s \equiv V_b - V_{TH} \equiv V_f + |V_{TH}| \equiv V_{DD} + V_{TH} = \min V_{DD} - |V_{TH}|
$$

$$
\Rightarrow \min V_{DD} = V_f + |V_{TH}| + |V_{TH}| \equiv 0.8 \sim 1.0V
$$

$0.54$ $-0.2$ $-0.3$

4. Measured results:

$V_{DD} : 2.2 \sim 4V$

$515 \pm 1mV$

$27^\circ C$

$85^\circ C$

$125^\circ C$

$515 \pm 3mV$

$\ast TC \equiv 60 \text{ ppm/}^\circ C \quad 27^\circ C \sim 125^\circ C$

Voltage drift (average) $\equiv 600 \mu V / V \quad 2.2V \sim 4V$
**CH 11 Digital-to-Analog Converters (DACs) in CMOS Technology**

§11-1 Introduction

1. Block diagram

![Block diagram of a typical signal processing system](image1)

(Digital signal processing has better noise immunity than analog signal processing.)

Fig. 11.1 A block diagram of a typical signal processing system

![Functional block diagram of a D/A converter](image2)

Fig. 11.2 Functional block diagram of a D/A converter
2. Ideal DAC:

Analog output signal \( V_{out} = V_{ref} \ (b_12^{-1}+b_22^{-2}+\cdots+b_N2^{-N}) \)

- \( V_{ref} \): analog reference signal
- \( b_1, \ldots, b_N \): N-bit digital data input

The signal change when one LSB changes is \( V_{LSB} \)

\[
V_{LSB} = \frac{V_{ref}}{2^N}
\]

If in LSB unit, \( 1LSB = \frac{1}{2^N} \)

3. DAC performance specifications

(1) Resolution: The number of distinct analog levels corresponding to the different digital words.

- N-bit resolution \( \rightarrow 2^N \) distinct analog levels.

(2) Offset error:

\[
E_{off(DAC)} = \frac{V_{out}}{V_{LSB}}|_{0\ldots0} \text{ (LSB)}
\]

(3) Gain error:

\[
E_{gain(DAC)} = \left[ \frac{V_{out}}{V_{LSB}}|_{1\ldots1} - \frac{V_{out}}{V_{LSB}}|_{0\ldots0} \right] - (2^N - 1) \text{ (LSB)}
\]
(4) Accuracy

absolute accuracy: The difference between the expected and actual transfer response. It includes the offset, gain, and linearity errors.

relative accuracy: The accuracy after the offset and gain errors have been removed.

⇒ maximum integrated nonlinearity (INL) error

*Accuracy units:

% of full-scale value.

effective number of bits

fraction of an LSB

*12-bit accuracy ⇒ all errors < 1 LSB \( \frac{V_{\text{out}}}{2^{12}} \)

(5) Integral nonlinearity (INL) error

Definition: The deviation of actual transfer response from a straight line.

INL error (best-fit) and INL error (endpoint)

Usually, INL error is referred to as the maximum INL error.
(6) Differential nonlinearity (DNL) error

Definition: The variation in analog step sizes away from 1 LSB.
(usually, gain and offset errors have been removed)

(7) Monotonicity: The output signal magnitude always increases as the input
digital code increases.

* Maximum DNL error $<\ 0.5\ \text{LSB} \Rightarrow \text{monotonicity}$
* Many monotonic DAC may have a maximum DNL error $>0.5\ \text{LSB}$
* Maximum INL error $<\ 0.5\ \text{LSB} \Rightarrow \text{monotonicity}$

(8) Settling time

The time it takes for the DAC to settle to within some specified
amount of the final value (usually 0.5 LSB)

(9) Sampling rate

The rate at which sample can be continuously converted.
(Typically the sampling rate is equal to the inverse of the settling time)

4. Types of DACs

(1) Decoder-based DAC
(2) Binary-weighted DAC
(3) Thermometer-code DAC
(4) Hybrid DAC
(5) Oversampling DAC
§11-2 Decoder-Based DAC

§11-2.1 Resistor-String DAC

1. Conceptual 8-bit resistor-string DAC.

2. Practical realization

   \( R_{0\ldots15} \): To divide \( V_{\text{REF}^+} \) to \( V_{\text{REF}^-} \) into 16 voltage intervals

   \( H_{0\ldots15} \)

   \( L_{0\ldots15} \): To divide each of those intervals into 16

   \( a \cdot p \) subintervals

   * To insure maximum uniformity of step size, i.e. linearity, the resistance
     of the transmission gates should be made as large as possible \( \Rightarrow \) minimal
     loading.

   * For 8-bit DAC, the error due to loading can be held to less than 1 LSB.

     if \( 16R_T > 2^N R_i \) \( (R_i = 200\Omega, R_T > 3.2K\Omega) \)
8-bit Resistor-String DAC (Multiple Resistor-String DAC)
Subinterval Generation:

* Transmission gate size: $24\mu/12\mu \rightarrow 3.2k\Omega = R_T$

* The raw speed of the DAC is limited by the resistance of transmission gates a-p and the capacitance of the output node, also by the operating speed of the output buffer.

* $V_{DD} = +5V$, $V_{SS} = -5V$, $Vout: \pm 2.5V$
  
  Maximum conversion rate $0 \square$ full scale : $2.5MHz$.

* For 8-bit DAC, the jump in step size can be held to less than 1 LSB if

$$16R_T \geq 2^N R_i$$

$$\frac{\Delta R_i}{R_i} = \frac{R_i - 16R_TR_i}{R_i + 16R_T} = \frac{R_i}{R_i + 16R_T} \leq \frac{1}{2^N}$$

$$\Rightarrow 2^N R_i \leq 16R_T \text{ occurs when } L_i=1$$
§11-2.2 Folded Multiple Resistor-String DAC

HIGH-SPEED DIGITAL-TO-ANALOG converters are usually designed with a current cell matrix. For resolutions higher than 8 bits required for new television standards, this approach requires either selection, trimming or calibration in the case of binary decoding, or accurate glitch matching and gradient compensation in CMOS if thermometer decoding is used. Moreover, many current-cell based circuits dump on average half of the current and often require the virtual ground of an external amplifier for optimum linearity with sufficient output drive.

This timeless 10-bit 50MHz D/A converter is based on resistor strings. The voltage dependence and the mutual matching of large-area polysilicon resistors allow the design of a converter with high integral and differential linearity. However, in a single 1024 resistor ladder output settling requires such low tap resistors that accurate resistor matching and consequently linearity becomes a problem.

The solution to this problem is the combination of a dual ladder with a matrix organization for the fine ladder, a full decoding scheme, an on-chip 75Ω output buffer and an additional ladder for the reduction of distortion at high signal frequencies. Figure 1 shows the ladder structure: the coarse ladder consists of two ladders each with 16 large-area 256Ω resistors connected in parallel to eliminate the first-order linearity gradient. The coarse ladder determines 16 accurate tap voltages. A 1024-resistor fine ladder is arranged in a 32-by-32 matrix, wherein every 64th tap is connected to the coarse ladder tap. There are currents in the connections between the ladders only in the case of ladder inequalities. This reduces the effect of contact resistance variance. The current density in the polysilicon is kept constant to avoid field-dependent non-linearities. In operation, the tap voltages of the fine ladder are switched to the 16 output rails of the matrix. The digital input word is decoded by two sets of 5-to-32 decoders followed by two groups of latches, as shown in Figure 2. At every tap an AND gate forms the final decoding. In each transition switch connects the ladder to the output rails, while another switch disconnects. This scheme minimizes ladder bounce caused by the switches, often observed in schemes where MSB decoding is combined with output rail multiplexing.

As the ladder of the D/A converter is designed for 2V unloaded output swing, second-order distortion will occur at high signal frequencies, due to the input-code-dependent switch drive voltage which causes signal-dependent RC time constants on the output rails. In this circuit, the drive voltage is kept constant by feeding the final AND decoding gates from an additional ladder: (Figures 1, 2). The total ladder configuration can now be fed from the 5V analog power supply. One external capacitor decouples the signal ladders. The clock feed through of the switches gives a linear signal contribution.

The multiplexer circuit at the end of the 16 output rails connects only the active rail to the output, keeping the other rails at the corresponding middle tap voltage. This scheme reduces the load capacitance and minimizes the recharging of the matrix output lines.

The output buffer is a folded cascode op amp where the output load is part of the output stage. The on-chip stop resistor allows a feedback path even for frequencies where the bondpad capacitance short the circuit output. The measured open-loop gain of the op amp into a 75Ω and 25pF load is 43dB with a unity gain bandwidth (UGBW) of 75MHz. (Figure 3).

Figures 4 and 5 show examples of performance with 75Ω and 25pF load. The lower side of the ladder is connected to give 0V input voltage. The overall integral linearity error is shown in Figure 4. The integral linearity is verified by measuring the distortion of low frequency input signals. The total distortion is less than 60dB.

The 10%-90% transition time is 6ns. (Figure 5) The extrapolated settling to within one LSB is about 20ns. The most critical glitch energy occurs for codes where the position is switched from the coarse ladder tap to the 32nd position on the corresponding fine ladder: in code: xxx000000 to xxx111111. The difference in glitch area is lower than 100pJ.

The D/A converter has been tested on computer-synthesized video pictures. Interference tests (9.6MHz input, 27MHz clock) confirm the linearity specifications. The effect of the additional supply ladder has been measured at 4.433MHz signal frequency and 50MHz clock rate. After the supply ladder is disconnected from the signal ladder and connected to the positive power supply, the total distortion increases by 10dB. At 50MHz clock rate, 125°C and a 130MHz signal frequency the distortion increases to about 40dB due to slew-rate limitations. Full-scale transitions have been measured up to a clock frequency of 100MHz, which shows the inherent speed of the ladder network.

Table 1 summarizes the performance. Power dissipation is measured with a full sine wave output signal, which consequently requires half of the top output current. Figure 6 shows a micrograph of the test chip.

---

**FIGURE 1**—Resistor network for the video D/A.

**FIGURE 2**—Block diagram of the D/A converter.

**FIGURE 3**—(a) Folded cascode op amp circuit used for the buffer; (b) Measured open-loop gain and phase on a 75Ω and 25pF load.

**TABLE 1**—Summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>1.4μm CMOS</td>
</tr>
<tr>
<td>DC resolution</td>
<td>10-bit</td>
</tr>
<tr>
<td>Differential linearity error</td>
<td>&lt;0.1 LSB</td>
</tr>
<tr>
<td>Integral linearity error</td>
<td>±0.6 LSB</td>
</tr>
<tr>
<td>Glitch energy</td>
<td>100ps V</td>
</tr>
<tr>
<td>Settling time (1 LSB)</td>
<td>20ns</td>
</tr>
<tr>
<td>Rise/Fall time (10%-90%)</td>
<td>6ns</td>
</tr>
<tr>
<td>Sample frequency</td>
<td>50MHz</td>
</tr>
<tr>
<td>Nominal power supply</td>
<td>5V</td>
</tr>
<tr>
<td>Output in 75Ω</td>
<td>1V</td>
</tr>
<tr>
<td>Power consumption (50MHz, 75Ω)</td>
<td>85mW</td>
</tr>
<tr>
<td>DAC size</td>
<td>2.5mm²</td>
</tr>
</tbody>
</table>

**FIGURE 5, 6**—See page 295
FIGURE 5—Photographs of the full-scale settling of the output.

FIGURE 6—Micrograph of the die.
§11-3 Binary-Weighted DAC

§11-3.1 Charge-Redistribution DAC

1. Multiplying DAC
   * All top plates are connected to the OP AMP input
     ⇒ To reduce substrate noise voltage injection.
   * Switched-induced errors are large.
   * Offset cancellation

2. Multiplying DAC with bipolar input

If \( b_0 = 0 \) ⇒ the signal \( V_{in} \) is positive
⇒ the same as 1.
If \( b_0 = 1 \) \( \Rightarrow \) the signal \( V_{\text{in}} \) is negative.

\[ \phi_1, \phi_2 \text{ positions are exchanged.} \]

\[ V_{\text{out}} = -V_{\text{in}} \sum_{i=1}^{n} b_i 2^{-i} \]

3. General characteristics or features of charge-redistribution DAC:

1. The auto-calibration cycle can be performed to remove the effects of component ratio errors.
2. Good linearity and stability due to good linear capacitors.
3. Too large capacitance ratio is required for high-bit DAC.
4. Suitable for medium-speed DAC with 6-bit resolution or below.

\section*{11-3.2 Weighted-Current-Source DAC (Current-Mode Binary-Weighted DAC)}

1. Conventional structure
   * Simple circuit structure without decoding logic.
   * At the mid-code transition 011---1 \( \Rightarrow \) 10---0, the MSB current source needs to be matched to the sum of all the other current sources to within 0.5 LSB.
     \( \Rightarrow \) difficult for large bit number.
     \( \Rightarrow \) not guaranteed monotonic.
   * Low-accuracy matching causes inaccurate bit transition
     \( \Rightarrow \) typical DNL plot as shown
   * The errors caused by the dynamic behavior of the switches, such as charge injection and clock feedthrough, result in glitches which is most severe at the midcode transition, as all switches are switching simultaneously.
     \( \Rightarrow \) contains highly nonlinear signal components
     \( \Rightarrow \) manifest itself as spurs in the frequency domain.

Conventional Weighted-Current-Source D/A Converter
Improved Structure

The Proposed 10-bit D/A Converter


1. Using Two-Stage Architecture:
   32 master & 32 slave current sources
   (Occupied small chip area but cause tight matching requirement
    among master current sources.)

2. Using Threshold-Voltage Compensated Current Sources
   to satisfy tight matching requirement.

   Only need local match &
   do not need global match.
Two-Stage Weighted Current Array D/A Converter
Conventional switched current source.

\[
I_1 = K \frac{W}{L} (V_a - V_{th1})^2 \\
I_N = K \frac{W}{L} (V_a - V_{thN})^2
\]

(V_{thN} - V_{th1}) may be as large as 80 mV due to the oxide thinning effect.
I_2 = K \frac{W}{L} (V_a - V_{th2})^2
= K \frac{W}{L} (V_{R1} + V_{thc} - V_{th2} + \sqrt{\frac{L_c I_c}{K W_c}})^2

1. \quad I_2 \gg I_c
2. \quad M_2 \text{ and } M_c \text{ are locally matched}

\Rightarrow I_2 = K \frac{W}{L} V_{R1}

Switched current source with threshold-voltage compensation.
Spice Monte-Carlo simulation results for (a) Conventional weighted current sources; (b) current sources with threshold-voltage compensation.
Two-stage weighted-current-source D/A converter with threshold-voltage compensated current sources.
(a) The circuit; (b) The SPICE simulated output waveforms of the input driver with high logic-threshold.
Symmetrical layout configuration of each 5-bit current array.

Different layout arrangement for the devices M2 and Mc in each current source: (a) 4-cell unit; (b) 5-cell unit.
Differential linearity error of the D/A converter
Integral linearity error of the D/A converter.
Differential and Integral linearity distribution of two kinds of layout methods for each current source.

<table>
<thead>
<tr>
<th>Linearity Error</th>
<th>4-Cell Unit(%)</th>
<th>5-Cell Unit(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 1/2 LSB</td>
<td>28.6</td>
<td>21.4</td>
</tr>
<tr>
<td>&lt; 1 LSB</td>
<td>82.1</td>
<td>67.9</td>
</tr>
<tr>
<td>&lt; 2 LSB</td>
<td>93.9</td>
<td>89.3</td>
</tr>
</tbody>
</table>

Characteristics of the D/A converter.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10 bits</td>
</tr>
<tr>
<td>Differential Nonlinearity</td>
<td>0.21 LSB</td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>0.23 LSB</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>125 MS/s</td>
</tr>
<tr>
<td>Settling Time (±1/2 LSB)</td>
<td>&lt; 8 ns</td>
</tr>
<tr>
<td>Rise/Fall time (10-90%)</td>
<td>3 ns</td>
</tr>
<tr>
<td>Glitch Energy</td>
<td>40 psV</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>150 mWatts</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>5V</td>
</tr>
<tr>
<td>Process</td>
<td>0.8um CMOS</td>
</tr>
<tr>
<td>Chip Size (without pads)</td>
<td>1.8mm×1.0mm</td>
</tr>
</tbody>
</table>

**SUMMARY**

1. Using threshold-voltage compensated current sources.
2. Two-step weighted current array 32 master, 32 slave unit current sources.
3. 10 bits, 125MHz, INL < ±0.21 LSB, DNL < ±0.23 LSB, 150mW.
§11-4 Thermometer-Code DAC

Current-mode thermometer-coded DAC; Current-cell-matrix DAC

1. Thermometer code (3 bit)

\[
\begin{array}{cccccccc}
 b_2 & b_1 & b_0 & d_6 & d_5 & d_4 & d_3 & d_2 & d_1 & d_0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\
 \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
\end{array}
\]

2. Conceptual circuit of thermometer-coded DAC

Advantages:

(1) Monotonicity is guaranteed.
(2) The matching requirement is much relaxed.

\[\text{e.g. } 50\% \text{ matching } \rightarrow DNL < 0.5 \text{ LSB}\]
(3) At the midcode transition the glitch is greatly reduced.

\[\text{only 1 LSB current source is switched.}\]
(4) Glitches do not contribute much to nonlinearity.

Glitches ∝ switched LSB
⇒ Glitch/LSB ≅ constant
⇒ Good linearity.

Disadvantage: Area consuming
□ Every LSB needs a current source, a switch, a decoding circuit, and the binary to thermometer decoder.

3. 8-bit current-mode thermometer-coded DAC

□ Conceptual architecture

* The two LSB bits D0 and D1 are fed to two parallel three-stage pipelined latches directly.

* The six MSB bits are fed to the decoders. (D2, -----, D7)
Segmented decoding structure of the DAC

Decoding scheme:

<table>
<thead>
<tr>
<th>Column</th>
<th>Row</th>
</tr>
</thead>
<tbody>
<tr>
<td>D4 D3 D2</td>
<td>D7 D6 D5</td>
</tr>
<tr>
<td>D4+D3+D2 = C1</td>
<td>D7+D6+D5 = R1</td>
</tr>
<tr>
<td>D4+D3 = C2</td>
<td>D7+D6 = R2</td>
</tr>
<tr>
<td>D4+D4+D3D2+D4D2 = C3</td>
<td>D7+D7D6+D7D5+D6D5 = R3</td>
</tr>
<tr>
<td>D4 = C4</td>
<td>D7 = R4</td>
</tr>
<tr>
<td>D4D3+D4D2 = C5</td>
<td>D7D6+D7D5 = R5</td>
</tr>
<tr>
<td>D4D3 = C5</td>
<td>D7D6 = R6</td>
</tr>
<tr>
<td>D4D3D2 = C7</td>
<td>D7D6D5 = R7</td>
</tr>
</tbody>
</table>

Decoding of current-source matrix:

<table>
<thead>
<tr>
<th>R1</th>
<th>R1+C1</th>
<th>R1+C2</th>
<th>R1+C3</th>
<th>R1+C4</th>
<th>R1+C5</th>
<th>R1+C6</th>
<th>R1+C7</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2</td>
<td>R2+R1C1</td>
<td>R2+R1C2</td>
<td>R2+R1C3</td>
<td>R2+R1C4</td>
<td>R2+R1C5</td>
<td>R2+R1C6</td>
<td>R2+R1C7</td>
</tr>
<tr>
<td>R3</td>
<td>R3+R2C1</td>
<td>R3+R2C2</td>
<td>R3+R2C3</td>
<td>R3+R2C4</td>
<td>R3+R2C5</td>
<td>R3+R2C6</td>
<td>R3+R2C7</td>
</tr>
<tr>
<td>R4</td>
<td>R4+R3C1</td>
<td>R4+R3C2</td>
<td>R4+R3C3</td>
<td>R4+R3C4</td>
<td>R4+R3C5</td>
<td>R4+R3C6</td>
<td>R4+R3C7</td>
</tr>
<tr>
<td>R5</td>
<td>R5+R4C1</td>
<td>R5+R4C2</td>
<td>R5+R4C3</td>
<td>R5+R4C4</td>
<td>R5+R4C5</td>
<td>R5+R4C6</td>
<td>R5+R4C7</td>
</tr>
<tr>
<td>R6</td>
<td>R6+R5C1</td>
<td>R6+R5C2</td>
<td>R6+R5C3</td>
<td>R6+R5C4</td>
<td>R6+R5C5</td>
<td>R6+R5C6</td>
<td>R6+R5C7</td>
</tr>
<tr>
<td>R7</td>
<td>R7+R6C1</td>
<td>R7+R6C2</td>
<td>R7+R6C3</td>
<td>R7+R6C4</td>
<td>R7+R6C5</td>
<td>R7+R6C6</td>
<td>R7+R6C7</td>
</tr>
<tr>
<td>R7C1</td>
<td>R7C2</td>
<td>R7C3</td>
<td>R7C4</td>
<td>R7C5</td>
<td>R7C6</td>
<td>R7C7</td>
<td></td>
</tr>
</tbody>
</table>
Logic diagram of the segmented row decoder

* Clocked CMOS gates
* Pipelined structure with two stages.

Logic diagram of the segmented column decoder is similar to that of the row decoder.

Current cell circuit

* The third stage of the pipelined circuit.
Symmetrical switching sequence to reduce the gradient effect.

- Current source and current switch
General characteristics/features of current-mode thermometer-coded DAC:

(1) No resistor or capacitor are used.

(2) Require special layout arrangement and complicated switching sequence to reduce the mismatches among current cells in the matrix ⇒ complicated decoder

(3) Logic circuits and long delay.

(4) Complicated wiring

(5) Large chip area ⇒ worse matching problem.

(6) Suitable for high-speed (video) and high-resolution (10-bit) CMOS DAC.

Current switching and better matching than resistors.
§11-5 Hybrid DAC

Combined architecture: Resistor-string + charge-redistribution DAC
Weighted-current-source + current-mode thermometer-coded DAC

§11-6 Case study


10-bit 500-MS/s CMOS DAC:

- Chip area comparison between weighted-current-source DAC and thermometer-coded DAC

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Binary Weighted</th>
<th>Thermometer Coded</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL (10-bit)</td>
<td>$(0.5\sqrt{1024})\sigma = 16\sigma$</td>
<td>$\sigma$</td>
</tr>
<tr>
<td>DNL (10-bit)</td>
<td>$\sqrt{1024}\sigma = 32\sigma$</td>
<td>$\sigma$</td>
</tr>
<tr>
<td>Area (INL=0.5-lsb)</td>
<td>$256*A_{\text{unit}}$</td>
<td>$256*A_{\text{unit}}$</td>
</tr>
<tr>
<td>Area (INL=1-lsb)</td>
<td>$64*A_{\text{unit}}$</td>
<td>$64*A_{\text{unit}}$</td>
</tr>
<tr>
<td>Area (DNL=0.5-lsb)</td>
<td>$1024*A_{\text{unit}}$</td>
<td>$A_{\text{unit}}$</td>
</tr>
</tbody>
</table>

$\sigma$: standard deviation of current sources.

$A_{\text{unit}}$: minimum required area to obtain a DNL = 0.5 LSB for the thermometer-coded architecture.

\[ \text{Chip area} \propto \frac{1}{\sigma^2} \]

- Normalized required chip versus percentage of segmentation and THD versus percentage of segmentation

\[ \Rightarrow \text{Optimal point} \]

$A_{\text{digital}} = A_{\text{INL}} = 1.0$ lsb

THD \[\Box\]
Block diagram: 8+2 segmentation

Cell circuit
Digital: decoding logic + latch
Analog: differential switch + cascoded current source.

Biasing scheme
Global biasing: common-centroid layout
Local biasing: 4 quadrants without direct connection between any two quadrants
⇒ DNL and INL
- Sinewave spectrum for Fs=300MS/s and Fsig=100MHz. SFDR=60dB

- SFDR versus Fsig/Fs

<table>
<thead>
<tr>
<th>SFDR</th>
<th>Fs(MS/s)</th>
<th>Fsig(MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>73dB</td>
<td>100</td>
<td>8</td>
</tr>
<tr>
<td>60dB</td>
<td>300</td>
<td>100</td>
</tr>
<tr>
<td>51dB</td>
<td>500</td>
<td>240</td>
</tr>
</tbody>
</table>
2. Definition of SFDR (Spurious-Free Dynamic Range)

SFDR: The signal-to-noise ratio when the power of the third-order intermodulation products equals the noise power.

\[ \text{SFDR} = \frac{I_{D1^*} - I_{D3^*}}{N_0} \] (dB)

- \( I_{D1} \) curve has a slope=1

\[ \Rightarrow \text{SFDR} = A_{I_{D3=N0}} - A_{N0}\left|_{I_{D1=N0}} \right. \]
§11-7 Summary


5. N. Kumazawa, N. Fukushima, N. Ono, and N. Sakamoto, "An 8 bit 150 MHz CMOS D/A converter with 2 Vp-p wide range output," 1990 Symposium on
VLSI Circuits, pp. 55-56.


16. Alex R. Bugeja, Member, IEEE, Bang-Sup Song, Fellow, IEEE, Patrick L. Rakers, Member, IEEE, and Steven F. Gilling, Member, IEEE "A 14-b, 100-MS/s CMOS DAC Designed for Spectral Performance," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 12, DECEMBER 1999.
CH 12 CMOS Analog Comparators

§12-1 General Considerations

Purpose of Comparators: To compare two input voltages and produce a very large output voltage with an appropriate sign to indicate which of the two is large.

Types of MOS Comparators:

A. Differential-input OP AMP

The latch provides a large and fast output signal, whose amplitude and waveform are independent of those of the input signal. Well suited for the logic circuits usually following the latch.

If no latch: -1mV $\square$ +1mV input = > -5V $\square$ +5V output

Gain = 5000, 74 dB

If use latch: The output voltage of A must be larger than the combined offset and threshold voltage of the latch, which is about 0.2V

= > Gain = 200

(1) Static configurations

(2) Dynamic configurations

B. Cascaded inverter stages

* Mostly dynamic
§12-2 Differential-Input OP AMP Comparators

§12-2.1 Static Configurations without Latches

1. * High Speed Comparator
   * Open loop gain: ~80dB
   * Output Swing: ±5V
   * Propagation Delay (±10mV Vin): ~1.2μs~2.4μs (15PF Load)
   * Generally, compensation circuit is not needed since there is no feedback connection.
   * Power Dissipation: ~10 mW

2. General-purpose comparators
   * Propagation delay: (±10mV, 15PF) 1.0μs~2.8μs
   * Power Dissipation: ~ 4mW
3. Comparator with level shift.

* Open loop gain: 60-80dB
* Output Swing: +5V → 0V
* Propagation delay (±10mV, 15 PF): 1.0μs~0.8μs
* Power Dissipation: ~1.5mW

4. CMOS Voltage Comparator MC 14574 (Motorola)

* Quad comparators
* Open loop gain (I_{set} = I_Q = 50\mu A): 96dB
* Propagation delay: ~1\mu s

5. Fully differential OP-AMP Comparators.

§12-2.2 Dynamic Configurations without Latches.

(1) Dynamic OP-AMP type comparator
* Compensated by C_2
* Vc1=Vin-Vos
* offset memorization

* \[ Vc1 = V_{ref} - Vin \]
* No compensation
* offset cancellation

\[ Vc1 \text{ and } V_{ref} \text{ are nonoverlapping clocks} \]
Practically, $\phi_{1a}$ must go low first in advance of $\phi_1$ to avoid the clock feedthrough effect of $S_1$ by $\phi_1$.

(2) Dynamic fully differential comparator

$C_1$, $C_2$: Autozeroing capacitors

$\phi_1 = 1$ \quad $V_{c1} = \text{Vin}^+ - \text{Vs}$, \quad $V_{c2} = \text{Vin}^- - \text{Vs}$

$\phi_2 = 1$ \quad $V_{c1} = \text{Vin}^+ - \text{Vin}^-$, \quad $V_{c2} = \text{Vin}^- - \text{Vin}^+$

$S_1$ and $S_2$ generate feedthrough voltages at $\Box$ and $\bigcirc$

$= >$ common-mode voltage

* CMRR can be promoted by using negative common-mode feedback circuit.
§12-2.3 Dynamic Configuration with Latches

Preamplifier-latch combination

Operating clock waveforms:

*\( \phi_2 \oplus 1, \quad S_5 \text{ short} = > Q_1, Q_2, Q_3, Q_4 \) and \( Q_7 \) are differential amplifier.

\( \overline{\phi}_2 \oplus 1, \quad S_6 \text{ short} = > Q_3, Q_4, Q_5, Q_6 \) and \( Q_7 \) are a bistable latch.
§12-3  Cascaded Inverter Stages

(1) Basic Structure

\[ V_{A1} = V_{in} + V_{A0} \]
\[ \Delta V_{A} = V_{in} \]

(2) CMOS Cascade Comparator.

* \( Q_1 \equiv Q_3, \ Q_2 \equiv Q_4 \)
* The speed of the cascaded inverter stages is limited by the RC times constants.

\[
R = R_0 = r_{dsP} || r_{dsn} \approx 100 \, \text{kΩ}
\]

\[
C_{in} = C_{gs} + C_{gd}(1 + |A|) \approx 0.5 \, \text{pF}
\]

\[A \approx 10\]

![Diagram of cascaded inverter stages](image)
(3) Fast comparators with two amplifiers and a single latch.

* Usually, the speed of a latch is faster than that of a amplifier.

=> Two amplifiers share one latch.

* Operating clock waveforms
§12-4 CMOS Dynamic Latches for Comparators

1. Direct-coupled latch with differential input signals

![Diagram of Direct-coupled latch]

* For single-ended inputs, Vin or Vin' may be replaced by a threshold voltage or can be generated by self-biasing

2. Capacitively coupled latch with autozeroing input

![Diagram of Capacitively coupled latch with autozeroing input]
\* \( \phi_2 \uparrow 1 \Rightarrow \) inverters \( Q_2-Q_5 \) and \( Q_3-Q_6 \) are biased at their optimal points. 

\( C_3 \) and \( C_4 \) are also precharged such that any asymmetry between the two inverters is compensated by the slightly different bias voltages provided by \( C_3 \) and \( C_4 \).

\[ \Rightarrow \] loop gain of the latch = 1.

\* \( \text{Vin}^+ < \text{Vin}^- : V_C \quad \text{H, } \quad V_D \quad \text{L.} \)

\( \text{Vin}^- < \text{Vin}^+ : V_C \quad \text{L, } \quad V_D \quad \text{H.} \)
§12-5 Case Studies

1. Differential-Input OP AMP Comparators with Dynamic Latches


\[ t_1 \sim t_2: \quad M_{12} \text{ ON} \ (\phi_2 = 1) \]
\[ M_{10} - M_{11} \text{ ON}, \ M_8 - M_9 \text{ OFF} \ (\phi_1 = 0) \]
\[ V_a = V_b, \ V_c = V_a, \ Q = \overline{Q} \]
\[ \text{Vin}_{\text{p1}} \text{ and } \text{Vin}_{\text{p2}} \text{ settles} \]
\[ t_2 \sim t_3: \quad V_a \neq V_b \text{ established with some regeneration of } M_4/M_5, \ M_{12} \text{ OFF} \]
\[ t_3 \sim t_4: \quad \phi_1 = 1, \ \phi_2 = 0 \quad \Rightarrow \quad M_{12} \text{ OFF}, \ M_{10}, \ M_{11} \text{ OFF}, \ M_8, \ M_9 \text{ ON} \]
\[ \text{strong regeneration} \quad \Rightarrow \quad V_c \neq V_a, \ V_a = V_c, \ V_b = V_d \quad \Rightarrow \quad Q, \overline{Q} \]

established

for input sampling

\[ t_1 \ t_2 \ t_3 \ t_4 \]
Performance:

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>1.5 µm CMOS</td>
</tr>
<tr>
<td>Die size</td>
<td>140 x 100 µm²</td>
</tr>
<tr>
<td>Power supply</td>
<td>+2.5 / -2.5 V</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Resolution</td>
<td>8 bits, 1LSB=9.8 mV</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>10.6 mV (&lt; 7 bits)</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>65 MHz</td>
</tr>
<tr>
<td>Offset voltage</td>
<td>3.3 mV</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>30 fF</td>
</tr>
</tbody>
</table>
¶13-1 Introduction

1. Functional block diagram of a A/D converter

2. Ideal A/D Converter (ADC)

\[ V_{in} \pm V_{x} = V_{ref}(b_{1}2^{-1} + b_{2}2^{-2} + \ldots + b_{N}2^{-N}) \]

\[ = \frac{V_{ref}}{2^{N}} (b_{1}2^{N-1} + b_{2}2^{N-2} + \ldots + b_{N-1}2^{1} + b_{N}2^{0}) \]

where \( V_{in} \) is the input analog voltage or current
\( V_{ref} \) is the reference voltage or current
\( b_{1} \ldots b_{N} \) is the digital output
\( V_{x} \) is the tolerable input signal range

\[ -\frac{1}{2}V_{LSB} \leq V_{x} \leq \frac{1}{2}V_{LSB} \]

2-bit ADC:

Input-output transfer curve:

- Offset by \( \frac{1}{2}V_{LSB} \)

\[ V_{LSB} = \frac{1}{4}V_{ref} \rightarrow 1 \text{ LSB} \]

\[ \frac{V_{LSB}}{V_{ref}} = \frac{1}{4} \rightarrow 1 \text{ LSB} \]

The input voltage or current should remain less than \( 3/4 V_{ref} + 1/8 V_{ref} = 7/8 V_{ref} \) and greater than \( 0 - 1/8 V_{ref} = -1/8 V_{ref} \).
Overloaded ADC: When $V_{\text{in}}>V_{\text{in|ideal}}+V_x$ or $V_{\text{in}}<V_{\text{in|ideal}}-V_x$, the quantization error is greater than $1/2 \, V_{\text{LSB}}$.

3. Quantization noise

Quantization error $\rightarrow$ Quantization noise.

$V_1 = V_{\text{in}} + V_Q$

$V_Q = V_1 - V_{\text{in}}$

Quantization noise modeling:

(1) Deterministic approach

$$V_{Q(rms)}(t) = \frac{1}{T} \left[ \int_{-\tau/2}^{\tau/2} V_Q^2 \, dt \right]^{1/2} = \frac{1}{T} \int_{-\tau/2}^{\tau/2} V_{\text{LSB}}^2 \left( \frac{t}{T} \right)^2 \, dt$$

$$= \left[ \frac{V_{\text{LSB}}^3}{T^3} \left( \frac{3}{3} \right) \left\{ \int_{-\tau/2}^{\tau/2} \right\} \right]^{1/2} = \frac{V_{\text{LSB}}}{\sqrt{12}}$$

(2) Stochastic approach

$$V_{Q(rms)}(t) = \left[ \int_{-\infty}^{\infty} x^2 f_Q(x) \, dx \right]^{1/2}$$

$$= \frac{1}{V_{\text{LSB}}} \left( \int_{-V_{\text{LSB}}/2}^{V_{\text{LSB}}/2} x^2 \, dx \right)^{1/2} = \frac{V_{\text{LSB}}}{\sqrt{12}}$$
4. Signal-to-Noise Ratio (SNR)

(1) $V_{in}$ is a sawtooth of height $V_{ref}$ (or a random signal uniformly distribut between 0 and $V_{ref}$)

$$\Rightarrow \text{SNR} = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log 2^N = 6.02 \text{ N dB}$$

(2) $V_{in}$ is a sinusoidal waveform between 0 and $V_{ref}$.

$$\Rightarrow \text{SNR} = 20\log\frac{V_{in(rms)}}{V_{Q(rms)}} = 20\log\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}} = 20\log\left(\frac{\sqrt{3}}{\sqrt{2}} \times 2^N\right) = 6.02 \text{ N +1.76 dB}$$

The above SNR is the best possible SNR for an N-bit ADC

$$V_{inpp} = V_{ref} \text{ (0 dB)} \rightarrow \text{SNR = 6.02 N +1.76 dB}$$

$$V_{inpp} \Rightarrow -20 \text{ dB} \rightarrow \text{SNR = (6.02 N +1.76) dB -20 dB}$$

5. Performance specifications

(1) Missing codes (equivalent to monotonicity in DAC)

Maximum DNL < 0.5 LSB or maximum INL < 0.5 LSB

$$\Rightarrow$$ The ADC is guaranted not to have any missing code.

(2) Conversion time

The time taken for the ADC to complete a single measurement including acquisition time of the input signal.

(3) Sampling rate

The speed at which samples can be continuously converted. Typically, the sampling rate is equal to the inverse of the conversion time except in the case of pipelining structure or multiplexing structure.

(4) Sampling-time uncertainty or aperture jitter

Due to the effective sampling time changing from one sampling instance to the next.

Sinusoidal waveform case:

$$V_{in} = \frac{V_{ref}}{2} \sin(2\pi f_{in} t)$$
\[
\frac{d}{dt} V_{\text{in}}\big|_{\text{max}} = \pi f_{\text{in}} t
\]

zero-crossing point

If \( \Delta V < 1 V_{\text{LSB}} \) for some sampling-time uncertainty \( \Delta t \),

\[
\Delta t < \frac{V_{\text{LSB}}}{\pi f_{\text{in}} V_{\text{ref}}} = \frac{1}{2^N \pi f_{\text{in}}}
\]

examples: 8-bit ADC, 250 MHz \( f_{\text{in}} \Rightarrow \Delta t < 5 \text{ ps} \)

16-bit ADC, 1 MHz \( f_{\text{in}} \Rightarrow \Delta t < 5 \text{ ps} \)

(5) Dynamic range

\[
\text{Dynamic range} = \frac{\text{r.m.s. value of the maximum input (output) sinusoidal signal}}{\text{r.m.s. value of the output noise plus the distortion when the same sinusoidal is present at the output}}
\]

It is also called the signal-to-noise-and-distortion ratio (SNDR).

* Can be expressed as effective number of bits using the SNR formula on p. 13-3.

* Input frequency dependent.

6. Types of ADCs

Low-to-medium speed: (1) Dual-slope or Integrating ADC
(2) Oversampling ADC
(3) Successive approximation ADC
(4) Algorithmic ADC

High speed: (1) Flash ADC
(2) Two-step ADC
(3) Pipelined ADC
(4) Interpolating ADC
(5) Folding ADC
(6) Time-interleaved ADC
§13-2 Successive-Approximation (SA) ADC's

§13-2.1 Resistor-string SA MOS ADC


Conceptual 3-bit unipolar ADC

Typical performance of a 8-bit ADC:

- p-type resistor: 100Ω
- Resolution: 8 bit
- Nonlinearity: $\pm \frac{1}{2}$ LSB
- DNL: $\pm \frac{1}{10}$ LSB
- Conversion time: 20 µs
- Input resistance: >1000 MΩ
- Stability (0° - 85°C): <1/4 LSB

Error Sources:

1. Resistor matching accuracy.

* Dividing the string into several equal lengths and locating them in close proximity.
2. The reverse bias junction voltage of the diffused resistors causes nonlinearity. 

\[ \text{Bit capacity} \uparrow \Rightarrow \Omega / \square \downarrow . \]

3. The small on resistance of the switches can decrease the settling time and reduce the feedthrough effect from the gate voltages. Similarly, the switch feedthrough only effects the settling time.

4. Major error source: The feedthrough in the switch transistor \( Q_2 \).

\[ 1 \text{ MHz clock} \rightarrow 2 \text{ mV error}. \]

5. Comparator offset error.

### §13-2.2 Charge-Balancing SA MOS ADC


* Mixed resistor string and binary-weighed cap.
13-bit ADC with laser-cut programmable Si-Cr fuse PROM's.

Post-process trimming => Linearity 1/2 LSB
Conversion Time 50 µs
Analog input - Vss ~ + Vcc
Clock freq. range 0.1 ~ 3MHz
Supply voltage ±4.5 ~ ±6.3V
Current drain 5mA

§13-2.3 Charge-Redistribution SA MOS ADC (CRSA ADC)

1. 10-bit CRSA ADC

Operation Procedures
(a) Sample Mode:

(b) Hold Mode:
(c) Redistribution (Approximation) Mode:

\[ S_1 \not= V_{\text{ref}}, \quad V_x = -V_{\text{in}} + \frac{V_{\text{ref}}}{2} \]

If \( V_x < 0 \), logic 1 in MSB (\( b_4 \)), \( V_{\text{in}} > \frac{V_{\text{ref}}}{2} \)

If \( V_x > 0 \), \( b_4 (\text{MSB}) = 0 \), \( V_{\text{in}} < \frac{V_{\text{ref}}}{2} \) and \( S_1 \not= \text{ground} \)

Final Configuration:

\[ V_x = -V_{\text{in}} + \frac{V_{\text{ref}}}{2} \left( \frac{b_4}{2^1} + \frac{b_3}{2^2} + \frac{b_2}{2^3} + \frac{b_1}{2^4} + \frac{b_0}{2^5} \right) = 0 \]

\[ V_x = -V_{\text{in}} + \frac{V_{\text{ref}}}{2^5} (2^4 b_4 + 2^3 b_3 + 2^2 b_2 + 2^1 b_1 + 2^0 b_0), \quad V_{\text{in}} > 0 \]
Complete ADC block diagram:

Measured Results:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10 bits</td>
</tr>
<tr>
<td>Gain error</td>
<td>&lt; 0.05 %</td>
</tr>
<tr>
<td>Linearity</td>
<td>$\pm \frac{1}{2}$ LSB</td>
</tr>
<tr>
<td>Sample mode acquisition time</td>
<td>2.3$\mu$s</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>0-10 V</td>
</tr>
<tr>
<td>Total conversion time</td>
<td>22.8 $\mu$s</td>
</tr>
<tr>
<td>Input offset</td>
<td>2mV</td>
</tr>
</tbody>
</table>
2. 12-bit modified CRSA ADC


* SAMPLE

* HOLD

* CHOOSE $V_{\text{ref}}$
Implement:

16 R, 8 ratioed capacitor, 37 MOS

R: S/D diffusion, 18Ω/□, 16 R= 9000 Ω

C: Unit capacitor, 400 µm², 0.1 pF

Measured data:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>12 Bits</td>
</tr>
<tr>
<td>Area</td>
<td>12,000 mil²</td>
</tr>
<tr>
<td>Monotonicity</td>
<td>12 Bits</td>
</tr>
<tr>
<td>Power dissipation (15V)</td>
<td>40 mW</td>
</tr>
<tr>
<td>Integral Linearity</td>
<td>6 Bits</td>
</tr>
<tr>
<td>DNL</td>
<td>1/2 LSB</td>
</tr>
<tr>
<td>Input. Offset</td>
<td>5 mV</td>
</tr>
<tr>
<td>Total conversion time</td>
<td>50µs</td>
</tr>
</tbody>
</table>

Operational Principle:

![Operational Principle Diagram](image)

<table>
<thead>
<tr>
<th>Sample</th>
<th>Hold</th>
<th>Choose V&lt;sub&gt;ref&lt;/sub&gt;</th>
<th>Discharge</th>
</tr>
</thead>
<tbody>
<tr>
<td>S&lt;sub&gt;A&lt;/sub&gt;</td>
<td>S&lt;sub&gt;B&lt;/sub&gt;</td>
<td>S&lt;sub&gt;1&lt;/sub&gt;</td>
<td>S&lt;sub&gt;2&lt;/sub&gt;</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(0)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-V&lt;sub&gt;in&lt;/sub&gt; + V&lt;sub&gt;ref&lt;/sub&gt;/4</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>-V&lt;sub&gt;in&lt;/sub&gt; + 2V&lt;sub&gt;ref&lt;/sub&gt;/4</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>-V&lt;sub&gt;in&lt;/sub&gt; + 3V&lt;sub&gt;ref&lt;/sub&gt;/4</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>Set up</td>
<td>1 (V_{ref})</td>
<td>2 (3V_{ref}/4)</td>
<td>OFF</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>----------------</td>
<td>-----</td>
</tr>
<tr>
<td>Redistribution</td>
<td>-V_{in} + (3/4)V_{ref} &lt; V_x &lt; -V_{in} + V_{ref}</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

\[ V_{in} + \frac{3V_{ref}}{4} + \frac{1}{8}V_{ref} \]

* The last capacitor C is always connected to B.
§13-3  Dual-Slope (Integrating; Charge-Balancing) MOS ADC's

$4\frac{1}{2}$ Digit ADC (Modified structure)
Waveforms observed at the node A:

NOTE: ENCLOSED AREA GREATLY EXPENDED IN TIME AND AMPLITUDE

Operational principles:

1. INT1
2. DE1

3. REST (INT2)

4. $\times 10$ (INT2)
5. DE2 (The same as DE1), $\Delta V'$: residual voltage

6. INT(ZI)

The final residual voltage $\Delta V'$ is effectively reduced to $\frac{1}{10}$ of the original residual voltage without amplification.

$\Rightarrow$ accuracy $\uparrow$
§13-4 Algorithmic ADC

Refs: 1. IEEE ISSCC, Digest of Papers, pp. 96-97, 1977

The conceptual block diagram of the algorithmic A/D converter

* The speed is limited by the settling time of OP AMPs used to implement the multiplier.
* For audio ADC applications, it could reach low-power low-voltage operation.
* Major error sources: (1) Capacitor ratio mismatches if SC circuits are used.
(2) Finite-gain error of OP amps.
(3) Offset voltage of OP amps.
(4) Capacitor feedthrough error by switches if SC circuits are used.
Complete circuit of the ratio-independent and gain-insensitive algorithmic ADCs

The complete circuit of the A/D converter

Clock waveforms:
Operational principles:

Step 1:

\[ V_y(1) \equiv \left( 2 - \frac{13A+20}{(A+2)^2} + \frac{13A+27}{(A+3)^2} \right) V_x(3) - \left( 1 - \frac{7A+8}{(A+2)^2} + \frac{7A+9}{(A+3)^2} \right) V_{\text{ref}} \]

Step 2:

\[ V_x(2) \equiv \frac{V_\text{in}}{1+2/A} \]

Step 3:

\[ V_x(3) \equiv V_\text{in} \left[ 1 - \frac{2}{(A^2+3A+2)} \right] \]
Step 4: 
\[ V_y(4) \equiv \frac{C_5}{C_6} (V_x(3) - V_{\text{ref}}) (1 + 3/A) \]

Step 5: 
\[ V_y(5) \equiv \frac{C_3}{C_4} (V_x(3) - V_{\text{ref}}) [1 + 6/(A^2 + 5A)] \]

Step 6:
Step 7:

\[
Vy(7) \approx \frac{(2 - \frac{2}{A+3})Vx(3) - (1 - \frac{2}{A+3})Vref}{1+3/A}
\]

Fully differential circuits:

The complete fully-differential circuit of the A/D converter
The folded-cascode fully-differential operational amplifier.

Chip photograph of the A/D converter.
A typical plot of the differential nonlinearity.

A typical plot of the integral nonlinearity.
A typical FFT plot of the A/D converter.

Table I  The Experimental results of the proposed A/D converter.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14 bits</td>
</tr>
<tr>
<td>Differential nonlinearity</td>
<td>&lt; ± 1/2 LSB</td>
</tr>
<tr>
<td>Integral nonlinearity</td>
<td>&lt; ± 1 LSB</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>10 KHz</td>
</tr>
<tr>
<td>Gain of op amp</td>
<td>60 dB</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>50 mWatts</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>± 2.5 V</td>
</tr>
<tr>
<td>Process</td>
<td>0.8 μm CMOS</td>
</tr>
<tr>
<td>Chip active area</td>
<td>2.1mm × 0.8mm</td>
</tr>
</tbody>
</table>
Table II  Comparison of the proposed A/D converter with the previous ratio-independent A/D converters [4.4]-[4.5].

<table>
<thead>
<tr>
<th>A/D converters</th>
<th>Performance</th>
<th>[4.4]</th>
<th>[4.5]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>(bits)</td>
<td>12</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td>Absolute</td>
<td>INL (LSB)</td>
<td>&lt;= 1.5</td>
<td>&lt;= 0.5</td>
<td>&lt;= 1</td>
</tr>
<tr>
<td>OP amp dc</td>
<td>Gain (dB)</td>
<td>92</td>
<td>84</td>
<td>60</td>
</tr>
<tr>
<td>Clock cycles</td>
<td>for n bits</td>
<td>6n</td>
<td>3n</td>
<td>7n</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>(KHz)</td>
<td>8</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>(mW)</td>
<td>17</td>
<td>-</td>
<td>50</td>
</tr>
</tbody>
</table>
§13-5 Full Flash (Parallel)

* Need $2^N$-1 comparators for N bits.
* Need $2^N$-1 Resister (R) tapes for N bits.
* S/H usually combined with comparators. (No op amp is required)
  
? Large no. of analog elements.

? Large chip area & power consumption.

Full-flash A/D converter
§13-5.1 MOS Flash ADC's


CMOS/SOS 6 bit 20 MHz ADC.

Block diagram of A/D converter chip.

High speed autozeroed CMOS/SOS comparator.
Discrete and distributed reference ladder models

\[ C_{\text{comp}} \leq 0.05 \text{ pF}, \quad R_{\text{TAP}} = 20 \Omega \]

\[ \frac{|Z(w)|}{R_{\text{TAP}}} \geq 50,000 \quad (< 10,000, \text{ don't work}) \]

Reference ladder leading as a function of input voltage

\(|Z(W)| / R_{\text{TAP}} = 500\)

Effect of loading ratio on reference ladder output.
Major source of error is the loading of the reference resistor ladder by the comparator bank.

Resistor ladder loading errors are of two types:

(1) "Transient error" associated with instantaneous ladder loading during a single measurement;

(2) Long-term "recovery error" associated with errors at a new input level after the ladder has been loaded for a long period by inputs at another level.

If the capacitor bypassing is performed at the externally accessible ladder midpoint tap,

⇒ transient impedance ↓ by a factor of more than 4.
⇒ Worst-case static loading which can't be bypassed makes recovery errors the significant error source.
* All the errors considered above are of this type.

Typical 6-bit A/D converter Performance:

Power dissipation at 15 MHz clock, 20 pF/output.

<table>
<thead>
<tr>
<th></th>
<th>5V</th>
<th>8V</th>
</tr>
</thead>
<tbody>
<tr>
<td>convert mode</td>
<td>50mW</td>
<td>145mW</td>
</tr>
<tr>
<td>Tracking mode</td>
<td>45mW</td>
<td>130mW</td>
</tr>
<tr>
<td>3.2V reference</td>
<td>9mW</td>
<td>9mW</td>
</tr>
<tr>
<td>Input Cap.</td>
<td>8 pF</td>
<td>8 pF</td>
</tr>
<tr>
<td>Recom. V&lt;sub&gt;ref&lt;/sub&gt;</td>
<td>3.2V</td>
<td>6.4V</td>
</tr>
<tr>
<td>On-chip Zener Reference</td>
<td>3.2V</td>
<td>6.4V</td>
</tr>
<tr>
<td>Input voltage source resistance</td>
<td>75Ω</td>
<td>75Ω</td>
</tr>
<tr>
<td>Accuracy 15MHz</td>
<td>$\frac{1}{2}$ LSB</td>
<td>$\frac{1}{2}$ LSB</td>
</tr>
<tr>
<td>20MHz</td>
<td>---</td>
<td>1 LSB</td>
</tr>
<tr>
<td>25MHz</td>
<td>---</td>
<td>1.5 LSB</td>
</tr>
</tbody>
</table>
§13-5.2 7-Bit CMOS Flash ADC for Video Applications


Overall schematic:

R: Polysilicon resistor, 10 Ω / bit

2μm Poly-gate VLSI CMOS

Overall ship area: 135×142 mil²
Comparator and the primary latch

Gain: 18dB
Bandwidth: 40 MHz

\( Q_{10}, Q_{13} \): Operated in linear region with on-chip low-power OP AMP and reference loop.
\[ \Rightarrow R_0 \downarrow, f_u \uparrow. \]

\( Q_{5}, Q_{6} \): Positive feedback to form latch.

\( Q_{11}, Q_{12} \): To limit the output swing and enable the comparator to recover much faster from the latched state.

The secondary latch is of the hysteresis type, because

(1) it can convert the limited logic swing of the primary latch to correct CMOS logic levels.

(2) it can reduce the amount of hysteresis to \(~ 100\) mV by setting "Latch"
signal to High. Thus the latch always experiences an overdrive of 100 mV.
⇒ Avoid ambiguous state and increase the resolution time of the comparators.
⇒ Reduce metastability error probability

Performance characteristics:
7-bit inherently monotonic
Accuracy: differential and integral \( \pm 0.5 \) LSB.
Analog bandwidth \( : -3 \text{dB} \ 42 \text{ MHz}; \ \frac{1}{2} \text{ LSB} \ 5 \text{ MHz} \)
Maximum sample rate \( : > 22 \text{ MSPS, 30 MSPS typically} \)
\( V_{DD} \) \( : \ 5V \pm 0.5V \)
Input range \( : \ 1.5V \sim 3.5V \)
Power consumption (25MSPS) \( : \ 350 \text{ mW} \)
Temp. range \( : \ -40^\circ \text{C to } +85^\circ \text{C} \)

\( \$13-5.3 \) CMOS 20 MS/S (Maga Samples /sec) 7-bit Flash ADC

Ref.: ISSCC 84, PP. 56-57, 315.

Nonsampling amplifier:
§13-5.4 **Metastability error**


Metastability error: occurs in ADCs when undefined comparator outputs pass through the encoder to the converter output bits.

* Metastability error rate is an exponential function of the sampling frequency.
* It is nearly independent of the input frequency.
* At 70-MHz sampling frequency, the metastability error rate is \( \sim 10^{-7} \) errors/cycle.
  \[ \Rightarrow 7 \text{ errors per second} \]
* Can be improved to \(< 10^{-12} \) errors/cycle.

![Diagram](image)

**Metastable state**

+ Thermometer code with valid comparator outputs
+ Thermometer code with metastable comparator

**Fig. 2.** Measured error rate versus sampling frequency for a 6-b CMOS flash converter with no error correction.
§13-6 Two-Step Flash or Subranging ADC

Conventional two-step A/D converter:

Two-step A/D converter with single resistor ladder:
Two-Step Flash ADCs or Subranging ADCs with:

(1) Two Resistor (R) Ladders
   * Need $2(2^{N/2}-1)$ comparators & R tapes.
   * Need high-performance op amp.
   ? Nonlinearity caused by the mismatch of the two resistor ladder.
   ? High-performance op amp is not easy to be achieved (especially for 3 V $V_{dd}$).

(2) Single Resistor Ladder
   * Need $2^N-1$ R tapes.
   * Need $2(2^{N/2}-1)$ comparators.
   ? As many R tapes as full flash type.
   ? No op amp is required.
§13-6.1 Subranging (Two-Step Flash) ADCs

8-bit 50MHz CMOS Subranging ADC with Pipelined Wide-Band S/H


Conventional subranging A/D converter:

![Subranging Diagram](image)

Trade-offs in Subranging and Flash 8-bit ADC

<table>
<thead>
<tr>
<th></th>
<th>Flash</th>
<th>Subranging</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total comparators</td>
<td>256</td>
<td>31</td>
</tr>
<tr>
<td>Clock cycles/conversion</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Relative speed</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>Relative input loading</td>
<td>1</td>
<td>0.12</td>
</tr>
<tr>
<td>Relative power dissipation</td>
<td>1</td>
<td>0.2</td>
</tr>
<tr>
<td>Relative die size</td>
<td>1</td>
<td>0.4</td>
</tr>
<tr>
<td>Typ. Differential Linearity Error</td>
<td>0.4 LSB</td>
<td>0.3 LSB</td>
</tr>
<tr>
<td>Typ. Integral Linearity Error</td>
<td>0.7 LSB</td>
<td>0.5 LSB</td>
</tr>
</tbody>
</table>

* High accuracy is required only for the S/H circuit and the D/A subconverter. (S/H is to reduce the effect of signal delay differences in the large-area chip.)

* Very difficult to develop a high-speed (video) and high-accuracy MOS S/H circuit.
* The conversion rate degrades. (Pipelined structure may be used)

* The linearity of the complete converter depends on the accuracy of the gain matching among the first A/D, the D/A, and the second A/D subconverters.

New structure: (4-bit conceptual structure)

Subranging A/D converter using combined DAC/subtraction technique: (a) block diagram and (b) subranging process

* Combined DAC/subtraction Technique
* No current flows through the switches ⇒ No degradation in linearity in DAC
* Amplifiers's settling time < 2 ns
8bit actual ADC:

![Block diagram of 8-bit subranging A/D converter](image)

* The 2\textsuperscript{nd} ADC has a fifth bit reserved for digital correction of nonlinearity caused by both offset voltages of the second S/H circuit and the subtractor and nonlinear errors in the first A/D subconverter.

* The two S/H circuits and two A/D subconverters operate in a pipelined manner ⇒ High conversion rate (≥ 2).

* The resistor string has more than 10-bit accuracy.

Gain Matching

![Linearity degradation caused by gain mismatches in pipelined S/H](image)
Conventional MOS S/H:

SF:
* The switch opening time is influenced by input voltages ⇒ severe distortion.
* Poor linearity.

Integrator-type S/H:
* The same switch closing time.
* Close loop configuration enhances the linearity.
* Difficult to obtain a fast-settling speed that ensures 8-bit accuracy.
Imposed by the relatively high output resistance of the amplifier and the clock feedthrough error of the MOS switch.

Conventional MOS S/H: (a) source follower type S/H, (b) waveform of clock \( \phi \) and switch opening time deviation for source follower S/H, and (c) integrator-type S/H

New S/H:

* Bandwidth-enhanced integrator-type S/H circuit.
* CMOS transmission gate with dummy transistor (clock feedthrough ↓)
* Compensation
\[
C_C = \frac{R_F}{R_1} C_H (1 + \frac{R_{SW}}{R_1} + \frac{R_{SW}}{R_F}) \quad \text{pole-zero cancellation.} \Rightarrow \text{Bandwidth} \uparrow.
\]
* \( C_I = 1 \) pF, \( C_C = 1.2 \) pF, \( R_f = R_i = 1 \) KΩ, \( R_{SW} = 100 \) Ω ⇒ 8-bit, 50 MHz.
\( T_{\text{settling}} = 12 \) ns ~ 8.5 ns for 2V step.
* The output of the subtractor is set to analog ground by closing the switch for the limiter.

**TABLE I**

**AMPLIFIER CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>53 dB</td>
</tr>
<tr>
<td>Unity Gain Frequency</td>
<td>380 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>60 degree(*)</td>
</tr>
<tr>
<td>Settling Time (AMP)</td>
<td>5.4 ns(*)</td>
</tr>
<tr>
<td>Settling Time (S/H)</td>
<td>8.5 ns(*)</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>83 mW</td>
</tr>
</tbody>
</table>

(*) Simulation
Comparators for the second A/D subconverter have an inaccuracy $\leq \frac{1}{4}$ LSB.

(3 mV at 3V input)

(FS)

* ≥ 100 MHz with a 7-8 mW power dissipation.
Timing diagram for pipelined subranging A/D converter

Experimental results:

1 μm CMOS, 5V single power supply, sampling rate 50 MHz.

Effective bits and gain as a function of analog input frequency

<p>| TABLE II |</p>
<table>
<thead>
<tr>
<th>CHIP PERFORMANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>Conversion rate</td>
</tr>
<tr>
<td>Effective bits</td>
</tr>
<tr>
<td>Effective resolution bandwidth</td>
</tr>
<tr>
<td>Input bandwith</td>
</tr>
<tr>
<td>Input capacitance</td>
</tr>
<tr>
<td>Power dissipation</td>
</tr>
<tr>
<td>Chip size</td>
</tr>
</tbody>
</table>
§13-6.2 10-bit 5-MSPS CMOS Two-Step Flash ADC


1. Classical two-step flash ADC
   * Limited by matching between the MSB ADC and DAC transitions
   * Limited by op-amp settling time (conversion rate)

Fig. 2. (a) Classical two-step flash ADC block diagram limited to bipolar technology. Limitations include matching the MSB ADC and DAC transitions otherwise missing codes and nonlinearity may result. (b) Timing diagram for the classical two-step flash ADC. Although the four phases are shown as equal length, the subtraction and gain are the slowest. They are limited by op-amp settling time and limit the conversion rate.

2. New structure
   * No OP amps.
   * No gain block

Fig. 3. Prototype subranging ADC block diagram. Notice that there are no op amps. The timing is similar to that in Fig. 2(b). The ADC's and DAC's share components to eliminate matching requirements among them.
3. Circuit implementation

<table>
<thead>
<tr>
<th>Problem</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Compatibility</td>
<td>5-V Operation</td>
</tr>
<tr>
<td>Power Supply Noise</td>
<td>Fully Differential Circuits</td>
</tr>
<tr>
<td>Charge Injection Errors</td>
<td>Fully Differential Circuits</td>
</tr>
<tr>
<td>Monotonicity</td>
<td>Cancel Comparator Offset</td>
</tr>
<tr>
<td>Fast, High-Gain Comparator</td>
<td>Multistage Comparator</td>
</tr>
</tbody>
</table>

* Shared binary weighted capacitor array for the MSB ADC and DAC and the LSB ADC.  
⇒ mismatches ↓

Fig. 4. Prototype converter’s MSB ADC and DAC. It operates like a standard CMOS flash converter. The 32-C capacitor is used as part of an S/H. It is a 5-bit array used for subranging in the LSB conversion. The DAC and ADC transitions match each other since the same resistor string is used for both.

Fig. 5. Prototype converter’s LSB ADC. Thirty-one ADC subsections each preset to codes 00001 through 11111 subdivide the region between $V_1$ and $V_2$ in the LSB’s flash decision. The ADC subsections are 5-bit binary-weighted capacitor-array ADC’s. The comparators, capacitors, latch bank, and encoder are the same ones used in the MSB ADC.
4. ADC Performance

**Table II**

**Prototype ADC PERFORMANCE AND SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Summary</th>
<th>10 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td></td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>5 Msamples/sec</td>
</tr>
<tr>
<td>Maximum DNL</td>
<td>0.6 LSB</td>
</tr>
<tr>
<td>Maximum INL (With comp.)</td>
<td>3.0 LSB</td>
</tr>
<tr>
<td>Maximum SNR (With comp.)</td>
<td>50 dB</td>
</tr>
<tr>
<td>Technology</td>
<td>1.6 μm CMOS</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>50 pF</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>350 mW</td>
</tr>
<tr>
<td>Area</td>
<td>54k mils²</td>
</tr>
</tbody>
</table>
§13-6.3 The Proposed A/D Converter

1. Parallel processing with two 8-bit subconverters. (Time-interleaved ADC)
2. Two-step structure with single resistor ladder.
   (No op amps is required)
4. 1-bit digital error correction.

- The proposed A/D converter with parallel processing architecture.
- The proposed 8-bit A/D subconverter.

![Diagram of the proposed 8-bit A/D subconverter]

- The timing diagram of a 8-bit A/D subconverter.

<table>
<thead>
<tr>
<th>Signal Type</th>
<th>Timing Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>ck1 (sample &amp; autozero)</td>
<td><img src="ck1-timing-diagram" alt="Timing Diagram" /></td>
</tr>
<tr>
<td>ck2 (fine comparison)</td>
<td><img src="ck2-timing-diagram" alt="Timing Diagram" /></td>
</tr>
<tr>
<td>Coarse comparator output</td>
<td><img src="coarse-comparator-timing-diagram" alt="Timing Diagram" /></td>
</tr>
<tr>
<td>Fine comparator output</td>
<td><img src="fine-comparator-timing-diagram" alt="Timing Diagram" /></td>
</tr>
<tr>
<td>Coarse encoder output</td>
<td><img src="coarse-encoder-timing-diagram" alt="Timing Diagram" /></td>
</tr>
<tr>
<td>Fine encoder output</td>
<td><img src="fine-encoder-timing-diagram" alt="Timing Diagram" /></td>
</tr>
<tr>
<td>Adder output</td>
<td><img src="adder-timing-diagram" alt="Timing Diagram" /></td>
</tr>
</tbody>
</table>
• The circuit of the coarse comparator.

• Fine comparator and its clock sequences.
- Intermeshed resistor reference ladder.
• The layouts and their equivalent circuits (a) with and (b) without separated unit resistors.

Experimental Results:
• Chip photograph of the fabricated A/D converter.
• A typical plot of the differential nonlinearity.

• A typical plot of the integral nonlinearity.
• The FFT spectrum for a 85 KHz sine-wave input signal

<table>
<thead>
<tr>
<th>SNR+D</th>
<th>SNR</th>
<th>THD</th>
<th>Peak Distortion</th>
</tr>
</thead>
<tbody>
<tr>
<td>46.87</td>
<td>47.98</td>
<td>-53.33</td>
<td>-63.78</td>
</tr>
</tbody>
</table>

-109.2 dB to 0 dB

• The effective bits versus input frequency characteristics.
Table 1 Major characteristics of the A/D converter.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process:</td>
<td>0.8µm CMOS</td>
</tr>
<tr>
<td>Resolution:</td>
<td>8bits</td>
</tr>
<tr>
<td>Differential nonlinearity:</td>
<td>-0.4 to + 0.4 LSB</td>
</tr>
<tr>
<td>Integral nonlinearity:</td>
<td>-0.6 to + 1 LSB</td>
</tr>
<tr>
<td>SNDR (for 85KHz input):</td>
<td>46.8 dB</td>
</tr>
<tr>
<td>Sampling rate:</td>
<td>50 MHz</td>
</tr>
<tr>
<td>Input dynamic range:</td>
<td>0.5V to 2.5V</td>
</tr>
<tr>
<td>Power supply:</td>
<td>3V</td>
</tr>
<tr>
<td>Power dissipation:</td>
<td>100 mW</td>
</tr>
<tr>
<td>Active area:</td>
<td>4950 um × 3790 µm</td>
</tr>
</tbody>
</table>
§13-7 Pipelined (Multistage) ADC

- Need $m(2^{N/m} - 1)$ comparators & R tapes.
- Need $m$ op amps for S/H & subtractors.
- High-performance op amp is not easy to be achieved (especially for 3V Vdd).

Block diagram of a pipelined A/D converter
Pipelined ADCs

§13-7.1 A Pipelined 5-Msps 9-bit ADC


1. General pipelined ADC

![Block diagram of a general pipelined A/D converter.]

2. Two-stage pipelined ADC

![Block diagram of a two-stage pipelined A/D converter with offset and gain errors.]

3. Prototype

![Block diagram of one stage in the prototype.]

Fig. 1. Block diagram of a general pipelined A/D converter.

Fig. 2. Block diagram of a two-stage pipelined A/D converter with offset and gain errors.

Fig. 5. Block diagram of one stage in the prototype.
Fig. 6. (a) Schematic of S/H amplifier. (b) Timing diagram of a two-phase nonoverlapping clock.

Fig. 8. Block diagram of A/D, D/A subsection.
Fig. 9. Connection of comparator with A/D, D/A subsection.

- OP AMP:

Fig. 7. Op-amp schematic.
Comparators:

4. Measurement results:

![Fig. 11. DNL versus code.](image1)

![Fig. 12. INL versus code.](image2)

![Fig. 13. SNR versus input level.](image3)

**TABLE I**

<table>
<thead>
<tr>
<th>Input Frequency</th>
<th>2 kHz</th>
<th>2 MHz</th>
<th>5.002 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak DNL (LSB)</td>
<td>0.5</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>Peak INL (LSB)</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
</tr>
<tr>
<td>Peak SNR (dB)</td>
<td>50</td>
<td>50</td>
<td>49</td>
</tr>
</tbody>
</table>

Data Summary over Input Frequency Variation
9-bit Resolution; 5-Msample/s Conversion Rate; ±5-V Power Supplies
§13-7.2 A Pipelined 9-Stage Video-Rate ADC


DAC + Σ + $\Rightarrow$ SHA ⇒ MDAC
Fig. 5 - Multiplying Digital-to-Analog Converter Schematic

Fig. 6 - Operational-Amplifier Schematic

Table 1 - ADC Performance: +5 V and 25°C

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.9-μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10 bits</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>20 Msamples/s</td>
</tr>
<tr>
<td>Area</td>
<td>9.3 mm²</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>300 mW</td>
</tr>
<tr>
<td>Input Offset</td>
<td>10 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.6 LSB</td>
</tr>
<tr>
<td>INL</td>
<td>1.1 LSB</td>
</tr>
<tr>
<td>SNDR (f_n = 100 kHz)</td>
<td>56.6 dB</td>
</tr>
<tr>
<td>SNDR (f_n = 5 MHz)</td>
<td>54.2 dB</td>
</tr>
<tr>
<td>DP</td>
<td>0.15 ° p-p</td>
</tr>
<tr>
<td>DG</td>
<td>0.23% p-p</td>
</tr>
<tr>
<td>PSRR (1 kHz)</td>
<td>55 dB</td>
</tr>
<tr>
<td>CMRR (5 kHz)</td>
<td>70 dB</td>
</tr>
</tbody>
</table>
§13-7.3 A Single-Ended 12-bit 20 MS/s Self-Calibrating Pipeline ADC


Advantages: concurrent processing of analog signals
⇒ optimal speed and power dissipation
⇒ high speed and low power

Disadvantage: * Inherent passive component matching problem
⇒ hard to control and yield ↓
⇒ self-calibration and correction technique
* Latency ⇒ acceptable in most applications

1. The pipeline architecture
* CMOS SC implementation
⇒ conversion stage speed
∝ feedback factor
∝ (interstage gain)^-1
⇒ 1-bit/stage for power and speed optimization.
⇒ simple calibration.

* Transfer characteristic:
The output residue voltage Vout
Vout = 2Vin + D Vref
D = +1 for 0 < Vin < Vref
= -1 for -Vref < Vin < 0

* Digital correction technique:
Very attractive for submicron CMOS (small chip area)
* The "radix = 2" overrange stage
  To correct residues up to $\frac{1}{2} V_{\text{ref}}$
  outside the nominal $\pm V_{\text{ref}}$ range for $V_{\text{in}}$.

Transfer characteristic:

$$V_{\text{out}} = 2V_{\text{in}} + 2 \cdot D \cdot V_{\text{ref}}$$

$$D = +1 \quad \frac{1}{2} V_{\text{ref}} < V_{\text{in}} < V_{\text{ref}}$$

$$= 0 \quad -\frac{1}{2} V_{\text{ref}} < V_{\text{in}} < \frac{1}{2} V_{\text{ref}}$$

$$= -1 \quad -V_{\text{ref}} < V_{\text{in}} < -\frac{1}{2} V_{\text{ref}}$$

Lower feedback gain for the overrange stage
⇒ maximum operating frequency ↓

* Overall architecture only 3 overrange stages are used for digital correction.

2. Self-calibration and correction algorithm
* Starting from the eleventh pipeline stage and working toward the MSB stage.
  The rest of the stages (12-15) are not calibrated.
* For each calibration stage, the calibration consists of
  (1) forcing an analog input value of 0V (differential)
  (2) forcing the digital decision to the left and to the right of the transition.
* The calibration coefficient
  \[ \text{Mem}_i = \text{code}_l - \text{code}_h \]
  \[ \text{Vout} = \text{Vref} \quad \text{Code}_l=0 \]
  \[ \text{Vout} = -\text{Vref} \quad \text{Code}_h=0 \]
  \[ \Rightarrow \text{Mem}_i = 2|\Delta \text{Vout}| = |\Delta \text{Vin}| \]

  one coefficient for regular stage.
  two coefficients for overrange stage.

  All the correction coefficients are stored in 15 registers.

* All the digital correction is performed in 16 bits, and the last 4 LSB’s are truncated for the final 12-bit output code.

* Global offset and full-scale error can be calibrated.

3. Implementation of Analog Blocks.

* The single-ended to differential input S/H:

![Block diagram of the single-ended to differential input S/H.](image-url)
* Input common-mode fb amp.

* op amp
  (telescopic op amp)

Fig. 8. Opamp circuit diagram, including output common-mode feedback.
4. Measurement results

DNL:

![DNL Plot]

Fig. 12. Typical DNL plot.

INL:

![INL Plot]

Fig. 13. Typical INL plot.
Spectrum:

Fig. 14. Spectrum for a single-ended 2-Vpp 1-MHz input sine wave.

SNR & THD

Fig. 15. Single-ended dynamic performance versus input frequency (20 Msample/s).
Fig. 16. Single-ended dynamic performance versus clock frequency (fin=1 MHz).

**TABLE I**

**Summary of ADC Performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample rate</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>INL</td>
<td>0.75 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.45 LSB</td>
</tr>
<tr>
<td>SNR (Nyquist)</td>
<td>65.4 dB</td>
</tr>
<tr>
<td>THD (Nyquist)</td>
<td>-72.6 dB</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>250 mW</td>
</tr>
<tr>
<td>Noise (rms)</td>
<td>0.36 LSB</td>
</tr>
<tr>
<td>Input range</td>
<td>0 to 2V</td>
</tr>
</tbody>
</table>
§13-8  Folding and Interpolating ADC


§13-8.1 Interpolating ADC

* The number of input amplifiers (or comparators as in flash ADC) attached to Vin can be significantly reduced by interpolating between adjacent output of these amplifiers.

A 4-bit interpolating ADC with interpolating factor of 4

* Transfer response of $V_1$, $V_{2a}$, $V_{2b}$, $V_{2c}$, $V_2$ vs. Vin: Logic 1 = 5V, Logic 0 = 0V
Gain of input amplifier = -10
Latch threshold = 2.5V
More reference levels between $V_1$ and $V_2$: $V_{2a}$, $V_{2b}$, $V_{2c}$. 
* If \( V_1 \) and \( V_2 \) are accurately linear between their own thresholds, i.e. \( 0.25V < V_{in} < 0.5V \)

⇒ correct crossing points of the latch threshold.

⇒ linearity ↑.

And the rest of the interpolated signal responses are of secondary importance.

* For fast operation, the delays of latches must be equalized by adding series resistors.

* Interpolation can be implemented by R string, current mirrors or capacitors.

Adding series resistors to equalize delay times to the latch comparators
§13-8.2 Folding ADC

A 4-bit folding ADC with a folding rate of 4.

* The use of a folding architecture to reduce significantly the number of latch comparators ($2^N$ in interpolating ADC).
* The use of analog preprocessing to determine the LSB set directly.
* Folding rate $\equiv$ the number of output transitions for a single folding block as $V_{in}$ is swept over its input range.
A folding block with a folding-rate of four. (a) A possible single-ended circuit realization; (b) input-output response.

* 4-bit folding ADC architecture:
  MSB 2-bit: flash
  LSB 2-bit: folding
  LSB: $V_1$, $V_2$, $V_3$, and $V_4$ produce a thermometer code for each of the four MSB regions.

* Examples: $V_{in}$:
  $0 \rightarrow 1/4$ V
  Thermometer code: 0000, 0001, 0011, 0111, 1111
  $V_{in}$: $1/4$ V $\rightarrow$ 1/2 V
  Thermometer code: 1110, 1100, 1000, 0000

* Total number of latches: 8
  as compared to 16 in flash ADC.

* No S/H is required.

* Folding blocks realized by BJT cross-coupled differential pairs as an example.

* Large input capacitance seen by $V_{in}$.

* The output signal frequency = input signal frequency $\times$ folding rate
  $\Rightarrow$ limits the practical folding rate used in high-speed converter.
§13-8.3 Folding and Interpolating ADC

A 4-bit folding A/D converter with a folding rate of four and an interpolate-by-two. (The MSB converter would usually be realized by combining some folding-block signals.)

* Folding rate: 4; Interpolation: 2
* $\overline{V_4}$ is a new inverted signal from $V_4$.
* Latch number ↓
  Input capacitance ↓
* Capable of > 100 MHz operation.
* Can be implemented in CMOS.
§13-8.4 A 400-Ms/s 6-bit CMOS Folding and Interpolating ADC


1. The structure of a folder with differential outputs.
   * A practical folder has
     5 amplifiers.

   ![Diagram of a folder with differential outputs](image1)

   ![Diagram of a practical folder](image2)

   ![Diagram of the differential outputs](image3)

   Fig. 2. (a) In this figure, a simple folder is highlighted. (b) A practical folder has an odd number of amplifiers. (c) The differential outputs are plotted.

2. A 3-bit folding converter and its cyclic code:
   * Folding rate $N$, full-scale sinusoid
     $\Rightarrow$ Folded signal frequency
     $\approx \frac{\pi}{2} N \cdot \text{frequency } F_{in}$

   ![Diagram of a 3-bit folding converter](image4)

   Fig. 3. A more complete diagram of a 3-bit folding converter.

   ![Diagram of the cyclic code](image5)

   Fig. 4. The figure shows the cyclic code generated by the two comparators. The 2-bit decoded binary value is also shown.
3. The block diagram of the 6-bit converter

![Block diagram of the 6-bit converter](image)

Fig. 5 Block diagram of the 6-bit converter

4. The folder structure:

![Folder structure](image)

Fig. 6. The folder is made of five two-stage amplifiers. The reference ladder is shared among all the folders.

* Folding rate: 4
  Interpolation: 2
* 16 comparators and 16 folders $\rightarrow$ cyclic thermometer $\rightarrow$ 5 LSBs.
* 5 amplifiers are used
* Two stages $\rightarrow$ higher gm.
* Resistor load $\rightarrow$ better transient performance.
* Output current mode $\rightarrow$ speed $\uparrow$. 
5. Practical folders:

![Diagram](image)

(a) The contribution of the fifth amplifier goes unused.
(b) This redundancy is used to reduce the number of preamplifiers

* Vx1 and Vx2 are fixed voltages generated by a single preamplifier shared by all folders.
* Power dissipation ↓.

6. Interpolation with current-mode folder signals

![Diagram](image)

Fig. 8. Interpolation can be used to eliminate half or more of the folder blocks

* The number of folders ↓. ⇒ 16 → 8

* Problems:   
  (1) It adds an extra node to the signal path, reducing the bandwidth of the folder circuit.
  (2) It does not work readily at low power supply voltages.
* Improved circuit:

Merge the current division within the folder.

![Diagram of a modified folder with current division](image1)

Fig. 10. The folder is modified to include current division. The modified amplifier is on the right. A block diagram for a modified folder is also shown.

* Fast operation and low-voltage operation.

7. Comparator design

(1) First stage:

![Comparator core diagrams](image2)

Fig. 12. The comparator core (a) tracking and (b) latching.

* Current-input voltage-output comparator.

* Resistor load.
* Advantages:

(a) Currents are summed to drive the latch (i.e. $I_{in_L} + I_{in_R}$) ⇒ The input signal has very little effect after latching begins.

(b) $I_{in_L}$ and $I_{in_R}$ always flow from tracking to latching ⇒ The folders are little disturbed.

* Need the second-stage buffer and latch.

(2) Second stage:

Fig. 13. Output voltage of comparator first stage during tracking and latching.

Fig. 14. Comparator second stage.
(3) Third stage to reduce metastability errors:

8. Complete ADC block diagram

The sync block: To suppress the delay mismatch between the coarse ADC and the rest of the circuitry (i.e. the fine converter)

* MSB-Lo and MSB-Hi are offset by $\frac{1}{8}$ Fs at either side of the MSB transition voltage.
* If MSB-1 = 0, MSB = MSB - Lo
  If MSB-1 = 1, MSB = MSB - Hi
* Can tolerate a relative offset of up to $\pm \frac{1}{8}$ Fs.
9. Measurement results:

Fig. 17. FFT for 1-MHz sinusoid sampled at 400 Msample/s (decimated).

Fig. 18. SNDR versus input frequency at 400 Msample/s

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<td>PERFORMANCE SUMMARY</td>
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Fig. 19. Die photo
§13-9 Summary

Resolution versus sampling frequency plot of recently reported CMOS audio A/D converters
Resolution versus sampling frequency plot of recently reported CMOS video A/D converters


CH 14. MOS Switched-Capacitor Filter Design

§14--1 Preliminary Considerations

§14-1.1 Classification of systems and filters

1. Continuous-time, discrete-time, and sampled-data systems

- Continuous-time system
  - e.q.: analog Filter
  - differential equations

- Sampled-data system
  - e.q.: SCF
  - difference equations

- Discrete-time system
  - e.q.: digital filter

2. Time-invariant systems and causal systems

- T.I. : \( x(kt) \rightarrow y(kt) \rightarrow x[(k-n)T] \rightarrow y[(k-n)T] \) for any \( x(kt) \) and \( n \).
- Causal : \( x(mt) \rightarrow y(kT) = 0 \) for \( k < m \)

3. Filter types:
   - (1) Low-Pass (LP)
     \[
     H(s) = \frac{K\omega_p^2}{S^2 + \left(\frac{\omega_p}{Q_p}\right)S + \omega_p^2}
     \]
     (biquad)
     Two complex poles (LHP)

\[ H(j\omega) \]
- \(-N*20\text{dB/decade}\)
- \(N: \text{order}\)
(2) High-Pass (HP)

$$H(s) = \frac{KS^2}{S^2 + (\omega_p/Q_p)S + \omega_p^2}$$

Two complex poles (LHP)
Two zeros at $$S=0$$

(3) Band-Pass (BP)

$$H(s) = \frac{K(\omega_p/Q_p)S}{S^2 + (\omega_p/Q_p)s + \omega_p^2}$$

center freq. gain: $$k$$
center freq. $$\omega_p$$
Two complex poles (LHP)
One zeros at $$S=0$$

(4) Band-Reject (BR)

$$H(s) = \frac{K(S^2 + \omega_z^2)}{S^2 + (\omega_z/Q_p)s + \omega_p^2}$$

$$\omega_p = \omega_z$$
Two complex poles (LHP)
Two imaginary zeros

$$\omega_p > \omega_z$$  High-Pass Notch filter (HPN)
$$\omega_p < \omega_z$$  Low-Pass Notch filter (LPN)

(5) Low-Pass Notch (LPN)

(6) High-Pass Notch
(7) ALL-Pass (Delay Equalizer)

\[
H(S) = \frac{S^2 - (\omega_p / Q_p)S + \omega_p^2}{S^2 + (\omega_p / Q_p)S + \omega_p^2}
\]

Two complex poles (LHP)
Two complex zeros (RHP)
mirror-imaged

§14-1.2 Sampling Process

§ ideal impulse sampling:

\[
S(t) = S_{\delta}(t) = \sum_{k=-\infty}^{\infty} S(t - k\tau)
\]

\(\tau\): sampling period

\[
x_d(t) = x(t)S_{\delta}(t) = x(t) \sum_{k=-\infty}^{\infty} \delta(t - k\tau) = \sum_{k=-\infty}^{\infty} x(t)\delta(t - k\tau)
\]

remember: \(\int_{-\infty}^{\infty} \delta(t - k\tau)dt = 1\) \(\delta(t - k\tau) = 0\) for \(t \neq k\tau\)

\(\Rightarrow x_d(t) = \sum_{k=-\infty}^{\infty} x(k\tau)\delta(t - k\tau)\)

Fourier transformation of \(S_{\delta}(t)\): \(S_F(t) = \sum_{k=-\infty}^{\infty} c_k e^{j \omega_k t}\)

\(\omega_k = \frac{2\pi}{\tau}\)

Where \(C_k = \frac{1}{\tau} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} s(t) e^{j \omega_k t} dt = \frac{1}{\tau}\)

\(\Rightarrow x_d(t) = x(t)S_F(t) = \sum_{k=-\infty}^{\infty} C_k x(t) e^{j \omega_k t}\)

\(F[x_d(t)] = F[\sum_{k=-\infty}^{\infty} C_k x(t) e^{j \omega_k t}] = \sum_{k=-\infty}^{\infty} C_k F[x(t) e^{j \omega_k t}]\)

\(= \sum_{k=-\infty}^{\infty} C_k X(j\omega - jk\omega_s)\) \(\text{where } F[x(t)] = X(j\omega), k = \pm\) integer

base-band spectrum
Sampling Theorem:
A function \( x(t) \) that has a Fourier spectrum \( X(j\omega) \) such that \( X(j\omega)=0 \) for \(|\omega| \geq \frac{\omega_s}{2} \) is uniquely described by a knowledge of its values at uniformly spaced time instants, \( \tau \) instants apart (\( \tau = 2\pi / \omega_s \))

\( 2\omega_c \): Nyquist rate.
Anti-aliasing filter is required.
Reconstruction filter is also required to recover \( x(t) \).

The smaller the \( \omega_s-2\omega_c \) (TB), the higher the filter order!

\[ |H(j\omega)| \]
§ Finite-Pulse Sampling (non-ideal sampling):

$$S_p(t) = \sum_{k=-\infty}^{\infty} [u(t - k\tau - \frac{a}{2}) - u(t - k\tau + \frac{a}{2})] \quad a > 0$$

$$C_k = \frac{1}{\tau} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} S_p(t) e^{-jk\omega_s t} dt$$

$$= \frac{1}{\tau} \int_{-\frac{\tau}{2}}^{\tau} e^{-jk\omega_s t} dt = \frac{a \sin(k\omega_s a/2)}{\tau k\omega_s / 2}$$

Now, we have $\sin \alpha / \alpha$ envelope onto $X(j\omega - jk\omega_s)$

$$\alpha \equiv k\omega_s a / 2$$

§14-1.3 Z-Transformation

$$x_d(t) = \sum_{k=-\infty}^{\infty} x(k\tau) \delta(t - k\tau)$$

Laplace Transformation $\Rightarrow$ $X_d(s) = L[x_d(t)] = \sum_{k=-\infty}^{\infty} x(k\tau) e^{-ks\tau}$

Let $z = e^{s\tau}$

$$S = j\omega \quad z = e^{j\omega \tau}$$

$X(z) = \sum_{k=0}^{\infty} X(k\tau) z^{-k}$ two-sided $z$-transform

$X(z) = \sum_{k=0}^{\infty} X(k\tau) z^{-k}$ one-sided $z$-transform

example 1: $x(t) = u(t) \Rightarrow x(k\tau) = 1 \Rightarrow X(z) = \sum_{k=0}^{\infty} z^{-k} = \frac{1}{1 - z^{-1}} \quad |z| > 1$

example 2: $x(t) = e^{-at} u(t) \Rightarrow x(k\tau) = e^{-ak\tau} \Rightarrow X(z) = \sum_{k=0}^{\infty} e^{-ak\tau} z^{-k} = \frac{1}{1 - e^{-a\tau} z^{-1}}$

For $|z| > e^{-a\tau}$

For single input/output, linear, time-invariant, sampled data (or discrete-time) system:

$$y(k\tau) + \sum_{n=1}^{N} b_n y[(k-n)\tau] = \sum_{n=0}^{M} a_n x[(k-n)\tau]$$

M.N: non-negative integers
Two cases:

(1) $b_n = 0$ for all $n$  $\implies$ nonrecursive system

M+1 tap transversal filter

Finite-Duration Impulse Response (FIR) Filter

(2) $b_n \neq 0$ for $n \geq 1$  $\implies$ Nth-order recursive system

Infinite Impulse Response (IIR) Filter

z-transform:

$$Y(z)(1+\sum_{n=1}^{N} b_n Z^{-n}) = X(z) \sum_{n=0}^{M} a_n z^{-n}$$

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{n=0}^{M} a_n z^{-n}$$

pulse transfer function

$$= \frac{a_1 (1-\beta_1 Z^{-1})(1-\beta_2 Z^{-1})...\cdots(1-\beta_N Z^{-1})}{(1-\alpha_1 Z^{-1})(1-\alpha_2 Z^{-1})...\cdots(1-\alpha_N Z^{-1})}$$

$z = \alpha_i$ : poles

$z = \beta_i$ : zeros

Mapping between Z-plane and S-plane:

$$z = e^{st} \Rightarrow z = e^{\sigma t} e^{j\omega}$$

$$\tau = \frac{2\pi}{\omega_s}$$

For $\omega_s > 2\omega_0$, the base-band response $X(j\omega)$ over the range $-\frac{\omega_s}{2} \leq \omega \leq \frac{\omega_s}{2}$ is sufficient to determine $X(j\omega)$ for all $\omega$.

* $-\frac{\omega_s}{2} \leq \omega \leq \frac{\omega_s}{2}$,  $-\infty < \sigma < \infty$  $\Rightarrow$ all Z-plane  $\angle Z = -\pi \rightarrow \pi$

* $-3\frac{\omega_s}{2} \leq \omega \leq -\frac{\omega_s}{2}$,  $-\infty < \sigma < \infty$  $\Rightarrow$ overlap on Z-plane  $\angle Z = -3\pi \rightarrow -\pi$

* $\frac{\omega_s}{2} \leq \omega \leq 3\frac{\omega_s}{2}$,  $-\infty < \sigma < \infty$  $\Rightarrow$ overlap on Z-plane  $\angle Z = \pi \rightarrow 3\pi$

* $\omega = \omega_1$,  $-\infty < \sigma < \infty$  $\Rightarrow$ a straight line from $z=0$ to $z=\infty$ with angle $\omega_1 \tau$

* j$\omega$ axis $\Rightarrow$ $\sigma = 0$  $\Rightarrow$ $|z|=1$ unit circle

* $\sigma > 0$  $|z|>1$ for all $\omega \Rightarrow$ RHP $\rightarrow$ outside the $|z|=1$ circle

* $\sigma < 0$  $|z|<1$ for all $\omega \Rightarrow$ LHP $\rightarrow$ inside the $|z|=1$ circle
First-order transfer function:
\[ H(z) = \frac{1}{1 - az^{-1}} \]
Z=a is the pole

\[ h(\tau) \quad k=0, 1, 2, 3, \ldots \]
\[ z=a = e^{\sigma \tau} e^{j\omega \tau} \]

(1) \( a>1 \), diverging unstable
(2) \( a=1 \) sequence of 1's unstable
(3) \( a \geq 0 \quad a<1 \) stable
(4) \(-1 < a \leq 0 \) stable \( \sigma<0 \), \( \omega \tau = \pm \pi \)
\( \omega k \tau = \pm k \pi \)
(5) \( a=-1 \) unstable
(6) \( a<-1 \) unstable

\[ G(\omega) = 20 \log |H(Z)|_{Z=e^{j\omega \tau}} \text{ dB} \quad \text{magnitude} \]
\[ \phi(\omega) = \tan^{-1} \left( \frac{\text{Im} H(Z)}{\text{Re} H(Z)} \right)_{Z=e^{j\omega \tau}} \text{ rad} \quad \text{phase} \]

The magnitude and phase can be determined graphically in the same way as those determined from the s-plane poles & zeros.

§14-1.4 Sample and Hold Circuit

Zero-order hold or S/H function:
\[ H_o(s) = \frac{1-e^{-s\tau}}{s\tau} \]
\[ H_o(j\omega) = e^{-j\omega \tau/2} \frac{\sin(\omega \tau/2)}{\omega \tau/2} \]
* may serves as a reconstruction circuit

\[ X_d(j\omega) = X_d(j\omega)H_o(j\omega) \]

* The difference between \( X_d(j\omega) \) & \( X_d(j\omega) \) at \( \omega \approx \pm \omega_c \) can be eliminated by setting \( \omega_s/\omega_c >> 1 \).

### §14-2 Switched-Capacitor Network System

General Switched-Capacitor Network (SCN):

- ideal capacitors, ideal voltage-controlled-voltage sources (VCVS's), ideal switches & sampled-data voltage inputs.
- VCVS: freq. indep. gain amps or infinite gain OP amps.

* Typically, the sampled-data voltage input is only single, not multiple.
* The input may be a continuous one.
* The effects of non-ideal switches, non-ideal OP amps, & non-ideal cap. should be considered as & second order effects.
Block diagram:

Switched-Capacitor Network
(Two-phase clock) (can be multi-phase)

General symbols:

$V_1(kT)$

$V_2(kT)$

$V_1(kT)$

$V_2(kT)$

$e$

$o$

$C$

$\phi$

$\phi^*$

$\phi^o$

$T_c < T$

to avoid overlapping of $\phi^*$ and $\phi^o$

$\tau$: sampling period

$\tau = 2T$

* Generally, SCN is time-variant since the network topology is different in the case of $\phi^*$ and $\phi^o$. However, if we separate the input/output sampled-data voltage into one even component and one odd component and separate the whole SCN into one even part and one odd part, then we have two time-invariant networks coupled together. Analysis thus can be performed.
Sampled-Data Waveforms

1. Return-to-zero waveforms

\[ V_a(z) = V^e_a(z) + V^0_a(z) = V^e_a(z) \quad V^0_a(z) = 0 \]

Similarly, we have \( V_b(z) = V^e_b(z) + V^0_b(z) = V^e_b(z) \quad V^0_b(z) = 0 \)

2. Full-clock-period (Full-cycle) sample-and-hold waveforms

\[ V_c(z) = V^e_c(z) + V^0_c(z) \]

\[ V^0_c(z) = Z^{-\frac{1}{2}} V^e_c(z) \quad (\therefore V^0_c(kT) = V^e_c([(k-1)T])) \]

Similarly, we have \( V_d(z) = V^e_d(z) + V^0_d(z) \)
\[ V_d^e(z) = Z^{-\frac{1}{2}} V_d^0(z) \]

Full-cycle S/H circuit

§14-3 Filter Design Process

1. Specification
   (1) Low-Pass Filter
      Specification:

[Diagram showing filter design process with specifications such as passband, stopband, transition band, and attenuation.]
2. Approximation
   (1) Classical approximation
       a. Butterworth
       b. Chebyshev
       c. Elliptic
       d. Bessel
   (2) Modern approximation

3. Realization
   Two methods:
   (1) Realization of the biquad (2\textsuperscript{nd} order filter) and the first-order filter $\Rightarrow$ cascade or couple them to form a high-order filter.
   (2) Realize $H(s)$ using LC network $\Rightarrow$ replace L by some integrated-circuit simulator or simulate the LC network using integrators.
       * Low-sensitivity, high-performance
§14-4 SC Integrators via OP AMPS

§14-4.1 SC Inverting Integrator

\[ \phi_o(\phi_e): V_{c1}=0 \]
\[ \phi_e(\phi_o): V_{c1}=V_1-V_2 \]
\[ \Delta Q=C_1(V_1-V_2) \]
\[ \frac{\Delta Q}{T}=i = C_1 \frac{V_1-V_2}{T} = C_1 f(V_1-V_2) = \frac{V_1-V_2}{R} \]
\[ \Rightarrow R = \frac{1}{C_1 f} \quad f: \text{clock frequency} \]
\[ \Rightarrow \text{SC simulated positive resistor} \]

Switch realizations:

The inverting SC integrator

\[ \phi_o \text{or} \phi_e \]

Operation:

(1) \( \phi_o \) phase
(2) $\phi_c$ phase

$$v_{in} \rightarrow v_{out}$$

$$v_{in} \rightarrow v_{out}$$

$$\phi_c$$

$$n-1 \quad n \quad n+1$$

$$t$$

$$V_{in}$$

$$V_{out}$$

$$v_{out}(T_n) \quad v_{out}(T_{n+1})$$

$$0V$$

$$v_{out}(T_{n-1}) \quad \frac{C_1}{C_2} (V)$$
"Ideal OP AMP"

\[
V_{\text{out}}(T_n) = V_{c2}(T_n) = V_{\text{out}}(T_{n-1}) - \frac{C_1}{C_2} V_{\text{in}}(T_n)
\]

\[
= \frac{V_{\text{out}}(T_n) - V_{\text{out}}(T_{n-1})}{T} = -\frac{C_1}{TC_2} V_{\text{in}}(T_n) = -\frac{1}{R_1C_2} V_{\text{in}}(T_n)
\]

\[
\Rightarrow \frac{d}{dt} V_{\text{out}} = -\frac{1}{R_1C_2} V_{\text{in}} = -\frac{1}{C_fC_2} V_{\text{in}} = \left(\frac{C_2}{C_1}\right)\left(\frac{1}{f}\right) V_{\text{in}}
\]

High-precision integrator time constant \( RC = \frac{C_2}{C_1} \frac{1}{f} \)

Z-domain Expression:

\[
V_{\text{out}}(z) = V_{\text{out}}(z)Z^{-1} - \frac{C_1}{C_2} V_{\text{in}}(z)
\]

\[
\Rightarrow H(z) \equiv \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = -\frac{(C_1/C_2)}{(1-Z^{-1})}
\]

Backward Euler Transformation: \( S \overset{1-Z^{-1}}{\rightarrow} T \)

\[
H(S) = -\frac{1}{(C_2/C_1)TS} = -\frac{1}{R_1C_2S}
\]

Parasitic-Free structure:
§14-4.2 Non-inverting SC Integrator

\[ \phi_e(\phi_o) : V_{c1} = +V_1 \]
\[ \phi_o(\phi_e) : V_{c1} = -V_2 \]
\[ \Delta Q = C_1(-V_1 - V_2) \]
\[ \frac{\Delta Q}{T} = i = -C_1 \frac{V_1 + V_2}{T} \]

If \( V_2 = 0 \)

\[ \Rightarrow i = -C_1 \frac{V_1}{T} = \frac{V_1}{R} \]
\[ \Rightarrow R = -\frac{T}{C_1} = -\frac{1}{C_1 f} \]

\[ \Rightarrow \text{SC simulated negative resistor!} \]

The non-inverting SC integrator:

Operations:

1. \( \phi_e \) phase

\[ \begin{align*}
V_{out}(T_n) &= V_{out}(T_{n-1}) + C_1 \frac{V_{in}(T_{n-1})}{C_2} \\
\Rightarrow \frac{d}{dt} V_{out} &= \frac{1}{R_1 C_2} V_{in}
\end{align*} \]

2. \( \phi_o \) phase

\[ \frac{V_{out}}{V_{in}}(s) \equiv H(s) = \frac{1}{R_1 C_2 S} = \frac{1}{C_1 f} S \]
Z-domain expression:

\[ H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{Z^{-1}\left(\frac{C_1}{C_2}\right)}{1 - Z^{-1}} \]

Forward Euler Transformation: \( S \rightarrow \frac{1-Z^{-1}}{TZ^{-1}} \)

\[ H(s) = + \frac{1}{\left(\frac{C_2}{C_1}\right)TS} = + \frac{1}{R_1C_2S} \]

- Simpler non-inverting integrator!

§14-5 Fully Differential-Type SC Integrators Using OP AMPs.

* Better noise rejection
* Better CMRR and PSRR
* Better Frequency response
* Better slew rate
** More components (switches, capacitor, OP AMPs)
** Thermal noise ↑ due to the added components and switching operations.
** Need common-mode feedback or common-mode bias circuit
§14-6 SC Differentiators Using OP AMPs

Inverting:

\[ V_{out}(T_n) = \frac{C_e}{C} \left[ V_{in}(T_n) - V_{in}(T_{n-1}) \right] \]

\[ H(z) = -\frac{C_i}{C} (1 - z^{-1}) \]

Backward-Euler Transformation: \[ S \rightarrow \frac{1 - z^{-1}}{T} \]

H(S) = \(-S \frac{C_i}{C} T = -S \frac{C_i}{C} \frac{1}{f} = -SRC_i \)

Noninverting:
Characteristics of SC differentiators:
1. Parasitic-free structure.
2. No dc instability problem as in SC integrators.
3. No high-frequency-noise problem as in continuous-time differentiators.
4. Can be used to design filters as SC integrators.

§14-7 The Design of SC Biquads (Second-Order Filter)

\[ H(S) = \frac{-(K_2 S^2 + K_1 S + K_0)}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} \]

§14-7.1 Low-Q SC Biquads

Step 1: Flow diagram generation.

\[ S^2 V_{\text{out}} = -(K_2 S^2 + K_1 S + K_0) V_{\text{in}} - (\omega_0 \frac{S}{Q} + \omega_0^2) \cdot V_{\text{out}} \]

\[ \Rightarrow V_{\text{out}} = -\frac{1}{S} [(K_1 + K_2 S) V_{\text{in}} + (\frac{W}{Q}) \cdot V_{\text{out}} + \omega_0 \cdot V_1] \]

where \( V_1 = \frac{1}{S} [(K_0 / \omega_0) \cdot V_{\text{in}} + \omega_0 \cdot V_{\text{out}}] \)

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<thead>
<tr>
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<th>[ - \frac{1}{S} ]</th>
<th>[ \frac{\omega_0}{Q} ]</th>
<th>[ - \frac{1}{S} ]</th>
<th>[ V_{\text{out}} ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ V_{\text{in}} ]</td>
<td>[ - \frac{K_0}{\omega_0} ]</td>
<td>[ \frac{1}{\omega_0} ]</td>
<td>[ \frac{1}{\omega_0} ]</td>
<td>[ V_{\text{out}} ]</td>
</tr>
</tbody>
</table>

\[ K_1 + K_2 S \]

Step 2: Active-RC design

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<tr>
<th>[ V_{\text{in}} ]</th>
<th>[ - \frac{\omega_0}{K_0} ]</th>
<th>[ C_A = 1 ]</th>
<th>[ - \frac{1}{\omega_0} ]</th>
<th>[ Q/\omega_0 ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ V_{\text{out}} ]</td>
<td>[ - \frac{1}{\omega_0} ]</td>
<td>[ \frac{1}{\omega_0} ]</td>
<td>[ \frac{1}{K_2} ]</td>
<td>[ C_B = 1 ]</td>
</tr>
</tbody>
</table>
Step 3: SCF

\[
C_1 = T \frac{K_o}{\omega_o} = |A_{dc}| \frac{\omega_o}{T} \frac{1}{x} 
\]

\[
C_2 = C_3 = \omega_o \frac{1}{x} 
\]

\[
C_4 = (\omega_o \frac{T}{Q}) \frac{1}{Qx} \iff \frac{Q}{\omega_o T} = \frac{C_A}{C_4} 
\text{ (not suitable for high Q)}
\]

\[
C_1' = K_1 \frac{1}{\omega_o x} 
\]

\[
C_1'' = K_2 
\]

\[
C_A/C_2 = \frac{1}{\omega_o T} 
\]

\[
X = \frac{1}{\omega_o T} 
\iff f_o = \frac{f_s}{2\pi x} \text{ } f_o: \text{ center (cutoff) frequency} 
\]

Step 4: refinement

Z-domain block diagram (If the accuracy is not good, change to Z-domain diagram)
In this diagram, each op-amp and its feedback capacitor (C_A or C_B) is replaced by its voltage-to-charge transfer function.

\[
\frac{Q_{out}(z)}{V_{in}(z)} = \frac{1/C_f}{1-z^{-1}} = \frac{V_{out}(z) \cdot C}{V_{in}(z)}
\]

Here C_f is the feedback capacitor.

Similarly,
- C \cdot (1-z^{-1}) for an unswitched capacitor (e.g. C_1")
- C for a non-inverting capacitor (C_1', C_3, C_4)
- -C \cdot z^{-1} for an inverting capacitor (C_1, C_2)

From the block diagram, the exact transfer function is

\[
\frac{V_{out}(z)}{V_{in}(z)} = - \frac{(C_1+C_2)z^2 + (C_1C_3 - C_1' - 2C_1'" - 2C_1' + C_2)z + C_1"}{(1 + C_4)z^2 + (C_2C_3 - C_4 - 2)z + 1}
\]

As compared to H(z) specifications, the capacitances can be determined.

\[
H(z) = \frac{-a_2\cdot z^2 + a_1\cdot z + a_0}{b_2\cdot z^2 + b_1\cdot z + 1}
\]

<table>
<thead>
<tr>
<th>TYPES</th>
<th>COEFFICIENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-P CASE</td>
<td>C_1&quot;=0  \quad K_1=K_2=0 \quad a_0=a_2=0</td>
</tr>
<tr>
<td>B-P CASE</td>
<td>C_1&quot;=0  \quad K_0=K_2=0 \quad a_0=0, a_1=-a_2</td>
</tr>
<tr>
<td>H-P CASE</td>
<td>C_1'=0  \quad K_0=K_1=0 \quad a_0=a_2=-\frac{a_1}{2}</td>
</tr>
<tr>
<td>NOTCH CASE</td>
<td>C_1'=0  \quad K_1=0 \quad a_2-a_0</td>
</tr>
</tbody>
</table>
§14-7.2 High-Q SC Biquads

\[ V_{out} = -\frac{1}{S} \left[ K_2 S V_{in} - \omega_0 V_1 \right] \]

Where \( V_1 = -\frac{1}{S} \left[ \left( \frac{K_0}{\omega_0} + \frac{K_1}{\omega_0} S \right) V_{in} + \left( \omega_0 + \frac{S}{Q} \right) V_{out} \right] \)

2. Active-RC design

3. SCF
$C_1 = K_0 \frac{T}{\omega_0} = (\frac{K_0}{\omega_0})\omega_0 T = |A_0| \omega_0 T$

$C_2 \cong C_3 \cong \omega_0 T$

$C_4 \cong \frac{1}{Q}$ (instead of $\frac{Q}{\omega_0 T}$)

$C_1' \cong K_1/\omega_0$

$C_1'' \cong K_2$

4. Z-domain block diagram of a high-Q biquad:

\[
\begin{align*}
\text{H}(Z) &= -\frac{C_1''Z^2 + (C_1C_3 + C_1'C_3 - 2C_1'')Z + (C_1''-C_1'C_3)}{Z^2 + (C_2C_3 + C_4C_4 - 2)Z + (1 - C_3C_4)} \\
\end{align*}
\]

Choose $C_2 = C_3$

Coefficient matching:

$C_1'' = \frac{a_2}{b_2}$

$C_1' = (C_1'' - \frac{a_2}{b_2})/C_3 = \frac{a_2 - a_3}{b_2c_3}$

$C_1 = (a_1/b_1 - C_1'C_3 + 2C_1'')/C_3 = (a_0 + a_1 + a_2)/(b_2c_3)$

$C_4 = (1 - \frac{1}{b_2})/C_3$

$C_3^2 = C_2^2 = (b_1/b_2 - C_3C_4 + 2) = (b_1 + b_2 + 1)/b_2$
§14-7.3 Design Examples

Example 1: Low-Q Lowpass SCF Biquad

\[
H(S) = \frac{4}{S^2 + 1.2S + 1}
\]

\begin{align*}
C_A &= C_B = 6.3 \\
C_1 &= 4
\end{align*}

\begin{align*}
C_2 &= 1 \\
C_3 &= 1 \\
C_4 &= 1.2
\end{align*}

\[
f_c = \frac{f_s}{2 \cdot \pi \cdot C_A} \\
f_s: CENTER FRE. \\
f_c: SAMPLING FRE.
\]

Example 2: Low-Q Bandpass SCF Biquad

\[
H(S) = \frac{4}{S^2 + 1.2S + 1}
\]

\begin{align*}
C_A &= C_B = 6.3 \\
C_1' &= 2
\end{align*}

\begin{align*}
C_2 &= 1 \\
C_3 &= 1 \\
C_4 &= 1.2
\end{align*}

\[
f_c = \frac{f_s}{2 \cdot \pi \cdot C_A} \\
f_c: CENTER FRE. \\
f_s: SAMPLING FRE.
Example 3: High-Q Low-pass SCF Biquad

\[ H(S) = \frac{4}{S^2 + \frac{S}{5.25} + 1} \]

\[ f_c = \frac{f_s}{2\pi C_A} \]

\( f_c \): CENTER FRE.
\( f_s \): SAMPLING FRE.

\[ C_A = C_B = 6.3 \quad C_1 = 4 \]

\[ C_2 = 1 \quad C_3 = 1 \quad C_4 = 1.2 \]

Example 4: High-Q Band-pass SCF Biquad

\[ H(S) = \frac{2S}{S^2 + 1.2S + 1} \]

\[ f_c = \frac{f_s}{2\pi C_A} \]

\( f_c \): CENTER FRE.
\( f_s \): SAMPLING FRE.

\[ C_A = C_B = 6.3 \quad C_1' = 2 \]

\[ C_2 = 1 \quad C_3 = 1 \quad C_4 = 1.2 \]
Frequency response of low-Q Low-pass SCF biquad

CENTER FREQUENCY: 1K Hz
SAMPLING FREQUENCY: 39.6 Hz

○ COMPUTED BY SWITCH CAP
× EXPERIMENTAL
Frequency response of low-Q Band-pass SCF biquad

CALCULATED

CENTER FREQUENCY: 1K Hz
SAMPLING FREQUENCY: 39.6 Hz

○ COMPUTED BY SWITCH CAP × EXPERIMENTAL
Frequency response of High-Q Low-pass SCF biquad

Center frequency: 1K Hz
Sampling frequency: 39.6 Hz

○ Computed by Switch Cap × Experimental
Frequency response of high-Q Band-pass SCF biquad

\[ 20 \log \left| \frac{V_{out}}{V_{in}} \right| \]

- CENTER FREQUENCY: 1K Hz
- SAMPLING FREQUENCY: 39.6 Hz

○ COMPUTED BY SWITCH CAP  × EXPERIMENTAL

FREQUENCY RESPONSE
§14-8 First-Order SCFs

\[ H_a(s) = -\frac{K_1S + K_0}{S + \omega_o} \quad H(z) = -\frac{a_1z + a_v}{b_1z + 1} \]

1. Flow diagram

2. Active-RC design

3. SCF

\[ C_1 \cong K_1 \]
\[ C'_1 \cong TK_0 \]
\[ C_2 \cong \omega_o T \]
\[ f_c = \frac{f_s}{2\pi x} \]
4. Z-domain block diagram

\[ H(z) = \frac{V_{out}}{V_{in}} = \frac{(C_1 + C_1')z - C_1}{(1 + C_2)z - 1} \]

\[ V_{out} = \frac{1}{C_2} \left( - \frac{V_{in}}{C_1(1-z^{-1})} \right) \]

---

§14-9 Switched-Capacitor Ladder Filters

§14-9.1 Approximate Design of SC Ladder Filters

(1) Third-order low-pass filter without finite transmission zeros

\[ -V_1 = -\frac{1}{SC_1} \left( \frac{V_{in} - V_1}{R_s} - I_2 \right) \]

\[ -I_2 = -\frac{1}{SL_2} (V_1 - V_3) \]

\[ V_3 = -\frac{1}{SC_3} (-I_2 + \frac{V_3}{R_L}) \]

---

Loss response

Loss

\[ \omega_p \]

\[ \omega \]

\[ => \infty \]

---

Flow diagram

LCR prototype circuit
SCF realization equations:

\[ C = \frac{T}{R} \quad \omega T << 1 \]

\[ \Rightarrow C_s \approx \frac{T}{R_s} \]

\[ C \approx T \]

\[ C_L \approx T / R_L \]

Due to the approximation made in finding C values, error still exists which may be refined by the z-domain analysis.
(2) Third-order low-pass filter with transmission zeros

\[ \omega_a = -\omega_{a2} = \sqrt{\frac{1}{L_2 C_2}} \]

\[-V_1 = \frac{-1}{s(C_1 + C_2)} \left[ \frac{V_{in} - V_1}{R_s} + sC_2 V_3 - I_2 \right] \]

\[-I_2 = \frac{-1}{sL_2} \left[ V_1 - V_3 \right] \]

\[+V_3 = \frac{-1}{s(C_2 + C_3)} \left[ -sC_2 V_1 - I_2 + \frac{V_3}{R_L} \right] \]

LCR Prototype circuit:

Flow diagram:
Active-RC Realization:

SCF:

\[ C_s \cong \frac{T}{R_s}, \]
\[ C_A = C_1 + C_2, \]
\[ C \cong T, \]
\[ C_B = L_2, \]
\[ C_c = C_2 + C_3, \]
\[ C_L \cong \frac{T}{R_L}. \]
(3) Fourth-order Bandpass filter

**LCR Prototype Circuit**

\[
\begin{align*}
-V_1 &= \frac{-1}{s(C_1 + C_2)} \left[ \frac{V_{in} - V_1}{R_S} + sC_2V_3 - I_1 - I_2 \right], \\
-I_1 &= \frac{-V_1}{sL_1}, \\
-I_2 &= \frac{-V_1 + V_2}{sL_2}, \\
V_3 &= \frac{-1}{s(C_2 + C_3)} \left[ -sC_2V_1 + I_3 - I_2 + \frac{V_3}{R_L} \right]
\end{align*}
\]
The circuit has a stability problem at dc.
Due to inductor loops!

\[ H_{AB} = \frac{V_B}{V_A} = \text{Circuits below} \circ \text{ and } \bullet \text{ disconnected} = \frac{-sL_i}{S^2 L_i (C_1 + C_2) + SL_i / R + 1} \]

\[ H_{CD} = \frac{V_C}{V_D} = \text{Circuits below} \circ \text{ and } \bullet \text{ disconnected} = \frac{-sL_j}{S^2 L_j (C_2 + C_3) + SL_j / R + 1} \]

When \( S \rightarrow 0, H_{AB} \rightarrow 0, H_{CD} \rightarrow 0 \)

\( \Rightarrow \) There will be no dc feedback paths around the center integrator which provides \(-I_2\).

\( \Rightarrow \) OP AMP will be in the open-circuit status with \( A \rightarrow \infty \).

\( \Rightarrow \) Saturation occurs

How to solve this problem?
Don't model the inductor loop currents separately.
i.e. \( I_1, I_2, I_3 \).
Only two inductive currents \( I_1 \) and \( I_2 \) entering nodes \( 1 \) and \( 3 \) are modeled.

\( \Rightarrow V_{in} = 0 \) and \( S \rightarrow 0, I_1 = 0 \) and \( I_3 = 0 \)

\( \Rightarrow \) No any instability at dc.
i.e.
Treat only two inductors as independent inductors.
\( I_1 = I_1 + I_2 \)
\( I_3 = I_2 - I_3 \)

New flow diagram:
-V₁ = \(-\frac{1}{s(C₁ + C₂)} \left[ \frac{V_{in} - V₁}{Rₙ} + sC₂V₃ - I_{(1)} \right],

- \dot{I}_₁ = - (I₁ + I₂) = \left( I₁ - \frac{L₁}{L₁ + L₂} \right) \left[ V₁ - \frac{L₁V₃}{L₁ + L₂} \right],

V₃ = \left( I₁ - \frac{L₁}{L₁ + L₂} \right) \left[ -sC₂V₁ - I_{(2)} + \frac{V₃}{Rₙ} \right],

- \dot{I}_₂ = \left( I₂ - \frac{L₂}{L₁ + L₂} \right) \left[ -V₃ + \frac{L₁V₁}{L₁ + L₂} \right],

Where \( L_{12} = \frac{L₁L₂}{L₁ + L₂} \)
SCF:
General Procedures for the approximate design of SC ladder filter:

1. A doubly terminated LC two-port is designed from the SCF specifications can be prewarped using the relation:

\[ W_a = \frac{2}{T} \sin \left( \frac{\omega T}{2} \right) \]

which represents the frequency transformation due to the LDI transformation implicit in the design produce.

Inverting SC integrator + Noninverting SC integrator

\[ H(z) = -\left( \frac{C_1 / C_2}_{inv} \right) \frac{(C_1 / C_2)_{noninv} z^{-1}}{1 - z^{-1}} \]

\[ = -K z^{-1} \frac{1}{(1 - z^{-1})^2} = \frac{-K}{(z^{1/2} - z^{-1/2})^2} \]

Ton \( z = e^{j\omega T} \)

\[ \Rightarrow H(e^{j\omega T}) = \frac{+K}{4 \sin^2 (\omega T/2)} \]

LDI mapping (Lossless discrete integrator):

\[ S_a = \frac{1}{2T} (z - z^{-1}) \]

If \( \frac{T}{2} \) is used \( \Rightarrow S_a = \frac{1}{T} (z^{1/2} - z^{-1/2}) \)

\[ \Rightarrow \omega_a = \frac{1}{T/2} \sin (\omega T/2) \]

2. The state equations of the LCR circuit are found. The signs of the voltage and current variables must be chosen such that inverting and noninverting integrators alternate in the implementation. If inductor loops exit, the inductive node currents can be used.
4. The block diagram or signal flow graph (SFG) is constructed from the state equations. It is then transformed (directly or via the active-RC circuit) into the SCF.

5. If necessary, additional circuit transformations can be performed to improve the response of SCF.

§14-10 Exact Design of SC Ladder Filters

* Ladder synthesis based on the bilinear $S_a$-to-$z$ transformation

\[ S_a = \frac{2}{T} \frac{z - 1}{z + 1} \quad \text{for} \quad \omega_a \text{-axis} \quad > \text{unit circle} \]

(1) preserves the flatness of PB and SB

§14-10.1 Third-order SCF (Low-pass with finite transmission zero)

\[
\begin{align*}
C_2' &= C_2 + C_{L2} \\
-C_{L2} &= -\frac{T^2}{4L_2}
\end{align*}
\]

\[-V_1 = \frac{-1}{S_a(C_1 + C_2')} \left[ -\frac{V_1 + V_{in}}{R_i} + s_a C_2' V_3 - I_2 \right],\]

\[-I_2 = \frac{s_a C_{L2}}{s_a L_2} \left[ V_1 - V_3 \right],\]

\[V_3 = \frac{-1}{s_a (C_2' + C_3)} \left[ -s_a C_2' V_1 - I_2 + \frac{V_3}{R_i} \right].\]

LCR Prototype Circuit:
Flow diagram

The center block has the transfer function:

\[ H(S_a) = S_a C_{L2} \cdot \frac{1}{S_a L_2} = \frac{1 - S_a^2 L_2 C_{L2}}{S_a L_2} = \frac{1 - (S_a T / 2)^2}{S_a L_2} \]

Transformation of the blocks into SC circuits:

1. Finding Q-V relations of all blocks and branches in the \( S_a \) domain.
2. Transforming the Q-V relations into the \( z \)-domain.
3. Realizing the transformed \( z \)-domain equations into SC circuits.

Five different blocks:

(a) The input branch \( \frac{1}{R_s} \)
\[ Q_{\text{in}}(S_a) = \frac{1}{R_s} V_{\text{in}} \frac{1}{S_a} \]

\[ Q_{\text{in}}(z) = \frac{T z + 1}{2} \frac{V_{\text{in}}(z)}{z - 1} \frac{1}{R_s} \]

\[ => (1-z^{-1})Q_{\text{in}} = \frac{T}{2R_s} (1+z^{-1})V_{\text{in}}(z) \]

\[ q_{\text{in}}(t_n)-q_{\text{in}}(t_{n-1}) = \frac{C_s}{2} [V_{\text{in}}(t_n)+V_{\text{in}}(t_{n-1})] \]

SC realizations:

Optional. To guarantee the charge flow only when \( \phi_1 = 1 \)

\[ \frac{C_s}{2} : \frac{C_s}{2} [V_{\text{in}}(t_n) - V_{\text{in}}(t_{n-1})] \]

\[ C_s : C_s V_{\text{in}}(t_{n-1}) \]

* Not stray insensitive.
  \( C_p + C_s \) not \( C_s \)

(b) The feedback branch \( \frac{1}{R_s}, \frac{1}{R_i} \)

\[ -\frac{C_s}{2} : -\frac{C_s}{2} [V_{\text{in}}(t_n) - V_{\text{in}}(t_{n-1})] \]

\[ C_s : C_s V_{\text{in}}(t_n) \]

\[ \frac{C_s}{2} [V_{\text{in}}(t_n)+V_{\text{in}}(t_{n-1})] \]

* Stray insensitive.

(c) The branches \( S_aC \)

\[ \frac{Q}{V} = CS_a \frac{1}{S_a} = C \]

Only a \( C \) is required.

(d) The blocks \( -\frac{1}{S_aC} \)

\[ \frac{Q}{V} = -C \quad => \text{OP with a feedback capacitor C.} \]
(e) The center block

$$I_2 = -\frac{1 - (S_a T/2)^2}{S_a L_2} (V_1 - V_3)$$

$$Q(S_a) = \frac{-I_2}{S_a} = -\frac{1 - (S_a T/2)^2}{S_a^2 L_2} (V_1 - V_3)$$

$$\Rightarrow \frac{Q(z)}{V_1(z) - V_3(z)} = -\frac{1 - [(z - 1)/(z + 1)]^2}{(4L_2 / T^2)[(z - 1)/(z + 1)]^2} = -\frac{4C_{L_2} Z}{(z - 1)^2}$$

$$\Delta Q(z) = (1 - z^{-1})Q(z) = \frac{4C_{L_2}}{z - 1} (V_3 - V_1)$$

$$\Delta Q(z) \frac{V_3 - V_1}{V_3 - V_1} = \frac{4C_{L_2} z^{-1}}{1 - z^{-1}} = (-Cz^{-1}) \left( -\frac{4C_{L_2}}{1 - z^{-1}} \right) (C)$$

Realizations:

The final realization is shown in the next page.

* This circuit is not fully stray insensitive.

* The negative capacitor $-\frac{C_A}{2}$ has been merged into the feedback capacitors $C_A$ and $C_B$, respectively.

$$C_A = C_1 + C_2' - \frac{C_s}{2} \quad \quad C_B = C_2' + C_3 - \frac{C_s}{2}$$

* Why $C_2'$, $-C_{L_2}$?

To create a block which is realizable by SC circuit.
The complete bilinear ladder circuit equivalent to the LCR circuit
14-10.2 Bandpass LCR filters

LC prototype Circuit:

-V2 can be produced as:

\[ I_2 = \left( S C_1 + \frac{1}{S L_1} \right) (V_1 - V_2) + \left( S C_3 + \frac{1}{S L_3} \right) (V_3 - V_2) - \frac{V_2}{S L_2} \]

Note that \( \frac{1 - (S_a T/2)^2}{S_a L} \) is realizable!

\[ = I_2(S) = S [(C_1 + C_{L1}) V_1 + (C_1 + C_3 + C_{L1} + C_{L3})(-V_2) + (C_3 + C_{L3}) V_3] \]

\[ + \left( \frac{1}{S} - \frac{T^2 S}{4} \right) [\Gamma_1 V_1 + (\Gamma_1 + \Gamma_2 + \Gamma_3)(-V_2) + \Gamma_3 V_3] \]

Where \( C_{L_i} \equiv \frac{T^2}{4L_i}, \Gamma_i = \frac{1}{L_i} \)

First Term:

\( Q_2'(S) = (C_1 + C_{L1}) V_1 + (C_1 + C_3 + C_{L1} + C_{L3})(-V_2) + (C_3 + C_{L3}) V_3 \)

Can be realized by unswitched capacitors.

Second Term:

\[ Q_2''(Z) = \left[ \frac{T}{2} \frac{z + 1}{z - 1} - \frac{T^2}{4} \right] [\Gamma_1 V_1 + (\Gamma_1 + \Gamma_2 + \Gamma_3)(-V_2) + \Gamma_3 V_3] \]

\[ = \frac{T^2 z^{-1}}{(1 - z^{-1})^2} [\Gamma_1 V_1 + (\Gamma_1 + \Gamma_2 + \Gamma_3)(-V_2) + \Gamma_3 V_3] \]
The same as before but now three functions are superposed together. \( \Delta Q_2''/V_1, \Delta Q_2''/(-V_2), \Delta Q_2''/V_3 \)

Conditions:

\[
\frac{C_4C_7}{C_8} = \frac{T^2}{L_1} = 4C_{L1}; \quad \frac{C_5C_7}{C_8} = T^2 \left( \frac{1}{L_2} + \frac{1}{L_3} \right) = 4(C_{L1} + C_{L2} + C_{L3})
\]

\[
\frac{C_6C_7}{C_8} = \frac{T^2}{L_3} = 4C_{L3}
\]

Stage providing \( Q_2''(z) \):

LC prototype circuit:

Design equations:

\[
C_{L1} = \frac{T^2}{4L_i}
\]

\[
c_1 = C_1 + C_{L1}
\]

\[
c_2 = C_1 + C_2 + C_3 + C_{L1} + C_{L2} + C_{L3}
\]

\[
c_3 = C_3 + C_{L3}
\]

\[
c_4 = 4 \frac{C_8}{C_7} C_{L1}
\]

\[
c_5 = 4 \frac{C_8}{C_7} (C_{L1} + C_{L2} + C_{L3})
\]

\[
c_6 = 4 \frac{C_8}{C_7} C_{L3}
\]

\[c_7, c_8\] arbitrary
LC prototype circuit with $R_S$:

\[ R_S \]

\[ C_1 \quad L_1 \]

\[ V_{in} \]

\[ V_2 \]

SC realization:

\[ V_{in} \quad c_1 \]

\[ c_2 \]

\[ c_3 \quad c_4 \]

\[ c_5 \quad c_6 \quad c_7 \]

\[ c_8 \quad c_9 \]

Design equations:

\[ C_{Li} \Delta T^2 \frac{T}{4L_i}, \quad C_S \Delta \frac{T}{R_S} \]

\[ c_1 = \frac{C_i}{2}, \quad c_2 = c_3 = C_9 \]

\[ c_4 = C_1 + C_2 + C_{L1} + C_{L2} - C_S/2 \]

\[ c_5 = 4 \frac{c_6}{c_7} (C_{L1} + C_{L2}) \]

\[ c_8 = C_2 + C_{L2} \]

\[ c_9 = 4 \frac{c_6}{c_7} C_{L2} \]

\[ c_6, c_7 \text{ arbitrary} \]
LC prototype

circuit with $R_L$:

SC realization:

Design equations:

\[ C_{L1} \frac{T^2}{4L_i}, \quad C_L \frac{T}{R_L} \]

\[ c_1 = C_1 + C_{L1} \]

\[ c_2 = 4 \frac{c_6}{c_7} \]

\[ c_3 = C_L \]

\[ c_4 = C_1 + C_2 + C_{L1} + C_{L2} - C_L / 2 \]

\[ c_5 = 4 \frac{c_6}{c_7} (C_{L1} + C_{L2}) \]

\[ c_6, c_7 \text{ are arbitrary} \]
Z-domain verifications:

Upper OP AMP:
\[ C_1(1-z^{-1})V_1 + C_3(1-z^{-1})V_3 + C_2(1-z^{-1})V_t + C_7V_b = 0 \]

Lower OP AMP:
\[-C_4z^{-1}V_1 - C_6z^{-1}V_3 - C_5z^{-1}V_t + C_8(1-z^{-1})V_b = 0 \]

\[ \Rightarrow \quad V_t = \frac{N_1 V_1 + N_2 V_3}{D} \]

\[ V_b = \frac{z^{-1}(1 - z^{-1})[(C_2C_4 - C_1C_5)V_1 + (C_2C_6 - C_3C_5)V_3]}{C_8D} \]

where

\[ N_1(z) = C_1C_8[(1-z^{-1})^2 + \frac{C_4C_7}{C_1C_8}z^{-1}] \]

\[ N_2(z) = C_3C_8[(1-z^{-1})^2 + \frac{C_6C_7}{C_3C_8}z^{-1}] \]

\[ D(z) = C_2C_8[(1-z^{-1})^2 + \frac{C_5C_7}{C_2C_8}z^{-1}] \]

* All poles and zeros of the transfer functions \( V_t/V_1, V_t/V_3, V_b/V_1, \) and \( V_b/V_3 \)
are located on the unit circle.

After the bilinear s-to-z transformation,

\[ V_t = \frac{S(1 - T)}{2} \left[ \left( \frac{C_1C_8 - C_4C_7}{4} \right) S^2 + \frac{C_4C_7}{T} \right] V_1 + \frac{V_3}{4} \left[ \left( \frac{C_3C_8 - C_6C_7}{4} \right) S^2 + \frac{C_6C_7}{T} \right] \]

\[ V_b = \frac{S(1 - T)}{2} \left[ \left( \frac{C_2C_4 - C_1C_5}{4} \right) S^2 + \frac{C_1C_5}{C_7} \right] V_1 + \frac{V_3}{4} \left[ \left( \frac{C_2C_6 - C_3C_5}{4} \right) S^2 + \frac{C_3C_5}{C_7} \right] \]

* The phase shift between \( V_t \) and \( V_1 \), as well as between \( V_t \) and \( V_3 \)
are either 0° or 180° for \( s = j\omega \)

\[ \Rightarrow \text{The same as for the LC prototype regardless of the} \]
element values \( C_i \).

\[ \Rightarrow \text{Can simulate a lossless LC with the same low} \]
sensitivity.
* It can also simulate the behavior of any LC ladder section which has a T configuration.

\[
\begin{align*}
\text{High-pass} & : V_t = -V_2 = V_2 \\
\text{Low-pass} & : V_t = -V_2
\end{align*}
\]

\[
V_2 = \frac{(aS^2 + b)V_1 + (cS^2 + d)V_3}{eS^2 + f}
\]

* High-Pass Case:

At \( Z = e^{j\omega T} = 1 \), i.e. \( \omega = \frac{2\pi}{2T} \),

If the loss is zero (i.e. passband),

\[
(1-z^{-1})Q_{in}(z) = \frac{T}{2R_s} (1+z^{-1})V_{in}(z)
\]

= 0

\( Q_{in}(z) = 0 \), but loss is zero

\( \Rightarrow \) The other part of the circuit should have an infinite gain.

\( \Rightarrow \) unstable.

\( R_s \) input (i.e. input termination) is a problem!

* Inductor loop is O.K.
§14-10.3 Comparisons

LDI Realizations of Ladder Filters using SC Integrators
(1) Prewarping is required
(2) Inductor loop exists
    => Modified design
    => Component sensitivity ↑

Bilinear Realizations of Ladder Filters using SC Integrations
(1) Prewarping is not required.
(2) Low-pass, band-pass ladder filters are O.K.
    But they are not fully stray insensitive.
(3) Can't realize high-pass or band-reject filters.
    => Instability exists.
(4) Some modifications are proposed.
    But they are not fully stray insensitive.

§14-11 The Scaling of High-Order SCF's.

Why scaling?
(1) Improve the actual performance.
(2) Reduce the silicon area
Let all branches connected to the output terminal of OA$_i$ be modified such that their $\Delta Q/V$ transfer functions $F_4$, $F_5$, and $F_6$ are multiplied by a positive real constant factor $k$. This can be achieved simply by multiplying all capacitors in these branches by $k_i$.

Since the input branches and their voltages were left unchanged, the change flowing in the feedback branch is

$$\Delta Q_4(z) = -\Delta Q_1(z) - \Delta Q_2(z) - \Delta Q_3(z)$$

remains at its original value.

$$=> V_2'(z) = \Delta Q_4(z) / [k_i F_4(z)] = V_i(z) / k_i$$

The new output voltage of OA$_i$ is the old output voltage of OA$_i$.

$$V_i \rightarrow V_i/k_i$$

due to scaling.

$$\Delta Q_5' = F_5'(z) V_i'(z) = k_i F_5(z) \frac{V_i(z)}{k_i} = F_5(z) V_i(z) = \Delta Q_5(z)$$

Voltage scaling does not change charge flowing from the scaled branch to the rest of the circuit.

$$=>$$ Only $V_i/k_i$, all other voltages or changes are not affected.

Optimization of the dynamic range using scaling

$$V_{\text{max}} / A_p \geq V_{\text{in, max}}$$

$A_p$: passband gain.
OA\(_2\) will saturate before OA\(_5\) because \(|V'_{2}| > |V'_{5}|\) for \(\omega \sim \omega_{2}\).

Now, we choose \(V_{in, max} = V_{max}/A_2\)

\[
A_2 = \frac{V_{p2}}{V_{in}}, \quad A_p = \frac{V_{p5}}{V_{in}}
\]

\[
A_2 = A_p \frac{V_{p2}}{V_{p5}}
\]

\[
V_{in, max} = \frac{V_{max}}{A_2} = \frac{V_{max}}{V_{p5}} \frac{V_{p5}}{V_{p2}} < \frac{V_{max}}{A_p}
\]

since \(V_p/V_{p2} < 1\)

\[\Rightarrow\text{Maximum } V_{in} \downarrow \Rightarrow \text{Dynamic range } \downarrow\]

Reducing \(V_2\) by scaling.

\[
V_2' = V_p(\omega)/k_2 \quad k_2 = V_{p2}/V_{p5}
\]

\[\Rightarrow V_2' \text{ has a peak value of } V_{p2}' \text{ which is equal to } V_{p5}.
\]

\[\Rightarrow V_{in, max} = V_{max}/A_p
\]

Similarly, \(k_3 = V_{p3}/V_{p5}, k_4 = V_{p4}/V_{p5} < 1\).

It is not good to choose \(k_2(k_3) > V_{p2}/V_{p5}(V_{p3}/V_{p5})\) because the noise will be increased.

\[\Rightarrow \text{dynamic range } \downarrow.
\]

CONCLUSION:

For maximum dynamic range, all op-amp outputs should be scaled such that each (at its own maximum frequency) saturates for the same input voltage level.
Let the transfer functions \( F_j(z) \equiv \Delta Q_j / V_j \) of all branches connected to the input terminal of OA\(_i\) be multiplied by a positive real constant \( M_i \Rightarrow C_i \rightarrow mC_i \)

\[
\Delta Q_n, \ n=1, 2, 3, 4 \rightarrow \Delta Q'_n = m_i \Delta Q_n
\]

\[
V'_i = \frac{\Delta Q'_4}{F'_4} = \frac{m_i \Delta Q_4}{m_i F_4} = \frac{\Delta Q_4}{F_4} = V_i \quad \text{V}_i \text{ unchanged!}
\]

The output charges \( \Delta Q_5 \) and \( \Delta Q_6 \) also remain the same

\( \Rightarrow \) The above scaling by \( m_i \) leaves all op-amp output voltages in the SCF unchanged. Only the charges in the scaled branches get multiplied by \( m_i \).

\( \Rightarrow \) Effective in reducing the cap. spread and the total capacitance of a SCF.

\( C_{i, \text{min}} \) among all capacitors contained in these four branches is located. \( \Rightarrow \) All capacitors contained in these four branches are multiplied by \( m_i = C_{\text{min}} / C_{i, \text{min}} \)

\( \Rightarrow \) The smallest capacitance becomes \( C_{\text{min}} \) and all op-amp voltages remain unaffected.

* Scaling for optimum dynamic range should be performed first, and scaling for minimum capacitance afterwards.

1. Scaling for Maximum Dynamic Range
   (a) Set \( V_{\text{in}}(\omega) \) to the largest value for which the output op-amp does not saturate. Record \( V_{\text{in}}(\omega) \) and \( V_{i, \text{max}} \)
   (b) Calculate \( V_{pi} \) for all internal op-amp output
   \( V_{pi} \) usually occur near the passband edges.
   (c) Multiply all capacitors connected or switched to the output terminal of op-amp \( i \) by \( \ k_i = V_{pi} / V_{i, \text{max}} \) where \( V_{i, \text{max}} \) is the saturation voltage at the output.
   (d) Repeat for all internal op-amps.

2. Scaling for Minimum Capacitance
   (a) Divide all capacitors in SCF into nonoverlapped sets.
   Capacitors in the \( i^{th} \) set \( S_i \) are connected or switched to the input terminal of
op-amp $i$.

(b) Multiply all capacitors in $S_i$ by $m_i=C_{\text{min}}/C_{i,\text{min}}$.

(c) Repeat for all sets $S_i$.

* Scaling for optimum dynamic range may also reduce the sensitivity to finite op-amp gain effects.

![Diagram of actual and equivalent circuits](image)

The influence of finite op-amp gain: (a) actual circuits; (b) equivalent circuits.

3. The block diagram or signal flow graph (SFG) is constructed from the state equations. It is then transformed (directly or via the active-RC circuit) into the SCF.

4. If necessary, additional circuit transformations can be performed to improve the response of SCF.
§14-10 Design Examples on Cascaded SCF and LDI Ladder SCF

§14-10.1 Cascaded SCF

Filter Specification
Passband: 0 to \( f_p = 1 \text{kHz} \)
  passband ripple \( \alpha_p \leq 0.05 \text{dB} \)
  (Maximum allowable passband gain variation)
Stopband: \( f_s \leq 1.5 \text{KHz} \) to \( f_c/2 \)
  Minimum stopband loss \( \alpha_s \geq 38 \text{dB} \)
  (Maximum allowable gain value)
Sampling frequency: \( f_c = \frac{1}{T} = 50 \text{KHz} \)

Design Procedures:
1. S-domain transfer function \( H(s) \)

Frequency prewarping
\[
\omega_{ap} = \frac{2}{T} \tan \left( \frac{\omega_p T}{2} \right) = 6291.4667 \text{ rad/s}
\]

Selectivity parameter
\[
k = \frac{\omega_{ap}}{\omega_{as}} \cong 0.6656
\]

Elliptic filter is chosen to minimize the filter order.

Results:
\[
\hat{H}(S_a) = \left( \frac{0.068}{S_a + 0.78140011 (-\tilde{a}_o)} \right) \left( \frac{S^2 a + \hat{\omega}_1^2}{S^2 a + 0.96934556 S_a + \hat{a}_1^2 + \hat{b}_1^2} \right) \left( \frac{S_a^2 + \hat{\omega}_2^2}{S_a^2 - 2\hat{a}_2 S_a + \hat{a}_2^2 + \hat{b}_2^2} \right)
\]

where \( \hat{a}_1 = -0.48467278, \hat{b}_1 = 0.82815049, \hat{a}_2 = -0.128006731, \)

\( \hat{b}_2 = 1.100351473, \hat{\omega}_1 = 1.5514948, \hat{\omega}_2 = 2.32131474 \)
The specifications are satisfied with \( \hat{\mathcal{H}}_a(0)=1 \)

2. frequency denormalization and z-domain transfer function \( H(z) \)

Denormalization:  \( S_a \rightarrow S/\omega_p \)

\[
\hat{\mathcal{H}}(S_a) \rightarrow \mathcal{H}(S) = K \frac{(S^2 + \omega_1^2)(S^2 + \omega_2^2)}{(S - a_o)(S^2 - 2a_1s + a_1^2 + b_1^2)(S^2 - 2a_2s + a_2^2 + b_2^2)}
\]

Where  \( K=428.247646, \omega_1=9.76117788 \times 10^3, \omega_2=1.46044744 \times 10^4, a_o=-4.91615278 \times 10^3 \)

\( a_1=-3.04930266 \times 10^3, b_1=5.21028124 \times 10^3 \)

\( a_2=-805.350086, b_2=6.92282466 \times 10^3 \)

Bilinear transformation:  \( S \rightarrow \frac{2z-1}{Tz+1} = 10^{15} \left( \frac{z-1}{z+1} \right) \)

\( \mathcal{H}(s) \rightarrow \mathcal{H}(z) = (C \frac{z+1}{z+d_o})(z^2 + C_1z + 1)(z^2 + C_2z + 1)
\)

Where  \( C=3.8719271 \times 10^3, C_1= -1.962247471, C_2= -1.916465445, d_o= -0.906284158, e_1= -1.871739343, f_1=0.88543246, e_2= -1.949416807, f_2=0.968447477. \)

Check:  \( |H(e^{j\omega T})| \) satisfies specifications.
3. SC realization

(1) \( H_0(z) = \frac{z + 1}{z - 0.9063} \)

\[ H_0(z) = -\frac{C_s/2}{C_D + C_E} \times \frac{z + 1}{z - C_E/(C_D + C_E)} \]

Cs = 2 arbitrarily chosen

\( =>C_E = 0.9063, \quad C_D = 0.0937 \)

(2) \( H_1(z) = \frac{z^2 + C_1z + 1}{(1/f_1)z^2 + (e_1/f_1)z + 1} \)

\( Q_1 = \frac{(a_1^2 + b_1^2)^{1/2}}{2|a_1|} \approx 0.99 \) Low-Q

The component values are:

\( C_1'' = a_0 = 1, \)
\( C_1' = a_2 - a_0 = 0, \)
\( C_2 = C_3 = \sqrt{b_1 + b_2 + 1} = \sqrt{(e_1 + 1)/f_1 + 1} \approx 0.12436, \)
$C_1 = (a_0 + a_1 + a_2)/C_3 \approx 0.30358,$
$C_4 = b_2 - 1 = 1/f_1 - 1 \approx 0.12939,$
$C_A = C_B = 1.$

\[ H_2(z) = \frac{z^2 + C_2 z + 1}{(1/f_2)z^2 + (e_2/f_2)z + 1} \]

\[ Q_2 = \frac{(a_2^2 + b_2^2)^{1/2}}{2|a_2|} \approx 4.33 \Rightarrow \text{High-Q} \]

The SCF is shown on P.14-23.

The component values are:
$C_1 = a_2/b_2 = f_2 \approx 0.96845, \quad C_1' = (a_1 - a_0)/b_2c_3 = 0,$
$C_2 = C_3 = \sqrt{(1+b_1+b_2)/b_2} = \sqrt{f_2 + e_2 + 1} \approx 0.13795,$
$C_1 = (a_0 + a_1 + a_2)/b_2C_3 = (2+c_2)f_2/C_3 \approx 0.58645,$
$C_4 = (1-1/b_2)/C_3 = (1-f_2)/C_3 \approx 0.22873.$

(4) Overall SCF

* Ho (low-pass linear section) is placed first
  =>$\text{High-frequency out-of-band signals and input noise can be attenuated.}$
  
  The antialiasing filter preceding the SCF has a lower requirement.
  
* H_2 (high-Q section) is placed to the center =>$\text{good signal-to-noise ratio}$
4. Scaling

1) $V_{p1}$ occurs at dc where $H_0(1) = -C_S/C_D = -21.345$

   (1) We want an overall passband gain of 1. $\Rightarrow H_0(1) \rightarrow -1$
   $\Rightarrow C_D = C_S = 2$, $C_E \approx 19.345$, $C_1 \approx 20.672$, $C_2 \approx 12.518$
   (Multiplying all capacitors connected or switched to the output node of op-amp $A_1$ by 21.345)

   (2) All capacitors at the input node of $A_1$ should be scaled so that the smallest ($C_S/2$) equals 1. (O.K.)

2) $V_{p2}$ (peak output voltage of op-amp $A_2$) occurs around $f_{p2} = 1.10$kHz

   (1) $V_{p2} \approx 177.05$ for $V_{in} = 1$

   Reducing $V_{p1}/V_{in}$ to 1

   $\Rightarrow C_A$ and $C_3$ are multiplied by 177.05 $\Rightarrow C_A \approx 177.05$, $C_3 \approx 24.424$.

   (2) $V_{p3} \approx 180.80$ at 1.07kHz

   $\Rightarrow C_B, C_2$, and $C_4$ are multiplied by 180.80 $\Rightarrow C_B \approx 180.80$, $C_2 \approx 24.941$, $C_4 \approx 41.354$.

3) Minimize total capacitance $\Rightarrow C_1, C_2, C_4$, and $C_A$ at the input node of op-amp $A_2$ are scaled to make $C_1 = 1$

   $\Rightarrow C_1 = 1$, $C_2 \approx 1.9926$, $C_4 \approx 3.3036$, $C_A \approx 14.144$

(4) Similarly, $C_1" = 1$, $C_3 \approx 1.1815$, $C_B \approx 8.7466$. (The input of $A_3$)

3) $V_{p4} \approx 503.57$ and $V_{p5} \approx 230.14$

   Thought the same procedures, we have

   $\overline{C_A} \approx 17.666$, $\overline{C_B} \approx 7.7286$

   $\overline{C_1} \approx 1.9926$, $\overline{C_2} = 1$

   $\overline{C_3} \approx 2.1116$, $\overline{C_4} = 2$

   $\overline{C_1} \approx 6.3085$

5 Final Design

$C_{min}$ is chosen as 0.5pF $\Rightarrow C = 1$

op amp: gain 70dB bandwidth 3 MHz

passband sensitivity to capacitance variation $\approx 0.2\text{dB}/1\%$

§14-12.2 Bilinear Ladder SCF Design

1. The same filter specification.

   Elliptic ladder filter is chosen (fifth-order).

   The result is
Normalized component values:

$\begin{align*}
R_s &= R_L = 1 \\
C_1 &= 0.85535 \\
C_2 &= 0.15367 \\
L_2 &= 1.20763 \\
C_3 &= 1.48438 \\
C_4 &= 0.46265 \\
L_4 &= 0.89794 \\
C_5 &= 0.63702 \\
\omega_{ap} &= 1 \text{ rad/s}
\end{align*}$

2. Frequency prewarping and denormalization

\[
\omega_{ap} \approx \frac{2}{T} \tan \left( \frac{\omega_p T}{2} \right) = 2 f_c \tan \left( \frac{\pi f_p}{f_c} \right) \approx 6291.4667 \text{ rad/s}
\]

Multiplying each resistor by $z_0$, each inductor by $L_0 = \frac{z_0}{\omega_{ap}}$, and each capacitor by $C_0 = \frac{1}{\omega_{ap}}$, we usually choose $z_0$ as the real source and termination resistance. Typically, we choose $z_0 = 50\Omega, 100\Omega, 600\Omega$.

Here, $C_0 = 1$ is chosen, so $z_0 = \frac{1}{\omega_{ap}}$ and $L_0 = \frac{1}{\omega_{ap}}$.

We have the denormalized element values as:

$\begin{align*}
C_1 &= 0.85535 \\
C_2 &= 0.15367 \\
L_2 &= 1.20763 \times L_0 = 3.05090 \times 10^{-8} \\
C_3 &= 1.48438 \\
C_4 &= 0.46265 \\
L_4 &= 0.89794 \times L_0 = 2.26851 \times 10^{-8} \\
C_5 &= 0.63702, R_s = R_L = z_0 = 1.58945 \times 10^{-4}
\end{align*}$

3. SC realization

Using the exact design technique of SC ladder filter (Section 14-10), the state equations are

\[
\begin{align*}
-V_1 &= -\frac{1}{sC_1'} \left( \frac{1}{R_s} (V_{in} - V_1) - I_2 + sC_2' V_3 \right), \\
-I_2 &= -\left( \frac{1}{sL_2} - sC_{L2} \right) (V_1 - V_3), \\
V_3 &= \frac{1}{sC_3'} (-I_2 - sC_{L2} V_1 - sC_4' V_5 + I_4),
\end{align*}
\]
\[ I_4 = \left( \frac{1}{sL_4} - sC_{L4} \right) (V_3 - V_5), \]

\[ -V_5 = \frac{1}{sC_5'} \left( I_4 + sC_4' V_3 - \frac{V_5}{R_L} \right), \]

where

\[ C_{L2} = \frac{T^2}{4L_2} = 0.003278, \]

\[ C_2' = C_2 + C_{L2} = 0.15695, \]

\[ C_1' = C_1 + C_2' = 1.01230, \]

\[ C_{L4} = \frac{T^2}{4L_4} = 0.0044082, \]

\[ C_4' = C_4 + C_{L4} = 0.46706, \]

\[ C_3' = C_3 + C_2' + C_4' = 2.10839, \]

\[ C_5' = C_5 + C_4' = 1.10408. \]

SCF:

arbitrarily chosen

\[ C = C_{L2} = 0.003278 \quad C' = C_{L4} = 0.004408 \]

\[ C_S = \frac{T}{R_S} = 0.1258293, \]

\[ C_A = C_1 + C_2 + C_{L2} - \frac{C_L}{2} = 0.94938, \]

\[ C_B = \frac{C_2}{4C_{L2}} = \frac{C_{L2}}{4} = 0.0008195, \]

\[ C_c = C_3 = 2.10839, \]

\[ C_D = \frac{C_4^2}{4C_{L4}} = \frac{C_{L4}}{4} = 0.001102, \]

\[ C_E = C_5' - \frac{C_L}{2} = 1.041165, \]

\[ C_L = \frac{T}{R_L} = 0.12583. \]
4. Scaling

\( V_{\text{in}} = 1 \text{V}, \) we have:

\[ V_{p1} \approx 0.92 \text{V}, \quad C_1 = 1.00000 \quad C_{05} = 1.14172 \]
\[ V_{p2} \approx 34 \text{V}, \quad C_2 = 1.83854 \quad C_{06} = 1.52861 \]
\[ V_{p3} \approx 0.764 \text{V}, \quad C_3 = 2.00000 \quad C_{07} = 2.02212 \]
\[ V_{p4} \approx 28.86 \text{V}, \quad C_A = 13.87171 \quad C_{08} = 1.00000 \]
\[ V_{p5} \approx 0.5 \text{V}, \quad C_{01} = 1.77112 \quad C_E = 8.27441 \]
\[ C_{02} = 1.20275 \quad C_D = 14.43078 \]
\[ C_{03} = 1.00000 \quad C_{04} = 1.00000 \quad C_{05} = 2.09575 \]
\[ C_B = 11.11901 \quad C_{06} = 5.67396 \]
\[ C_{07} = 1.46156 \quad C_{08} = 1.29480 \quad C_{09} = 1.90667 \]

for dynamic range scaling

minimum-capacitance scaling: \( \frac{C_A}{C_B} = 13.87171 \)

5. Final design

\( C_{\text{min}}, \quad \text{OP amp: 70dB 3 MHz} \)

=> Passband ripple: 0.06dB  minimum stopband loss \( \leq 39.5 \text{dB} \)

Maximum sensitivity: 0.05dB/

\section*{14-12.3 LDI Ladder SCF Design}

1. LCR prototype circuit

Fifth-order elliptic LC ladder filter with the same lowpass specifications.

2. Frequency prewarping and denormalization

\( \omega_{ap} \approx \omega_p \) (for simplicity)

\( z_0 = 1 \Omega \Rightarrow C_0 = \frac{1}{(2\pi 10^3)^2}, L_0 = \frac{1}{(2\pi 10^3)^2} \)

The denormalized element values:

\( R_s = 1 \Omega, \)
\( C_1 = 136.13318 \mu\text{F}, \quad C_4 = 73.633034 \mu\text{F}, \)
\( C_2 = 24.45734 \mu\text{F}, \quad L_4 = 142.91159 \mu\text{H}, \)
\( L_2 = 192.20028 \mu\text{H}, \quad C_5 = 101.38488 \mu\text{H}, \)
\( C_3 = 236.24641 \mu\text{F}, \quad R_L = 1 \Omega. \)

State equations:

\[ -V_1 = \frac{1}{s(C_1 + C_2)} \left( -\frac{V_1 + V_{in}}{R_s} + sC_2 V_3 - I_2 \right), \]
\[ -I_2 = \frac{V_1 - V_4}{sL_2}, \]
\[ V_3 = -\frac{1}{s(C_2 + C_3 + C_4)} \left( -I_2 - sC_2 V_1 - sC_4 V_5 + I_4 \right), \]
\[ I_4 = \frac{V_3 - V_5}{sL_4}, \]
\[ -V_5 = -\frac{1}{s(C_4 + C_5)} \left( I_4 + sC_4 V_3 - \frac{V_5}{R_L} \right). \]
3. SCF design

The flow diagram is shown on P.14-? whereas the active-RC circuit is given on P.14-?.

The SCF is shown on P.14-? where \( T = 20 \mu s \) is chosen and the component values are

\[
\begin{align*}
C_1 + C_2 &= 160.59 \mu F, \\
C_2 + C_3 + C_4 &= 334.34 \mu F, \\
C_s &= \frac{T}{R_s} = 20 \mu F, \\
C_4 + C_5 &= 175.018 \mu F, \\
C &= \frac{T}{I} = 20 \mu F, \\
C_L &= \frac{T}{R_L} = 20 \mu f
\end{align*}
\]

4. Scaling

Dynamic range scaling with \( V_{p_i} \) listed:

followed by minimum-capacitance scaling

for \( A_1: V_{p_1} = 0.927 \) V at 1.182 kHz.

for \( A_2: V_{p_2} = 1.198 \) V at 1.121 kHz.

for \( A_3: V_{p_3} = 0.857 \) V at 1.061 kHz.

for \( A_4: V_{p_4} = 1.105 \) V at 1.061 kHz.

for \( A_5: V_{p_5} = 0.501 \) V at 967 kHz.

Element values:

\[
\begin{align*}
C_1 &= 8.03214, \\
C_1 &= 12.97271, \\
C_{1A} &= 1, \\
C_{1B} &= 1.07930, \\
C_{1C} &= 1.29263, \\
C_{1D} &= 1.13212, \\
C_2 &= 13.42236, \\
C_{2A} &= 1.08053, \\
C_{2B} &= 1, \\
C_3 &= 8.75121, \\
C_{3A} &= 2.20614, \\
C_{3B} &= 1, \\
C_{3C} &= 6.29664.
\end{align*}
\]

5. Final design

\( C_{min} \) Passband ripple: 0.095dB>0.044dB

Minimum stopband loss: 40.5dB

OP amp: 70dB, 3MHz

Maximum passband sensitivity: 0.08dB/%
§14-13 Nonideal Effects in Switched-Capacitor Filters

1. Switch Turn-On Resistance

The turn-On resistance of a MOSFET can be written as

$$R_{on} = \frac{1}{2 \mu C_w w (V_{gs} - V_T)}$$

*Nonlinear behavior

The $R_{on}$ effect on the simple SC integrator:

At $t = nT$, $V_1(t) = V_1(nT) = V_{in}(nT)(1 - e^{-T/2RC_1})$

Assume $\phi_1$ and $\phi_2$ are activated for $T/2$.

$$\Delta Q(nT + \frac{T}{2}) = C_1 V_1(nT)(1 - e^{-T/2RC_1}) = [V_{out}(nT+T) - V_{out}(nT)]C_2$$

Let $R_1 = R_2 = R$

$$\Rightarrow H(z) = \frac{-(1 - e^{-T/2RC_1})^2 C_1}{z - 1} C_2$$

Ideal: $$H(z) = \frac{C_1}{z - 1} C_2$$
Error: \[ \varepsilon = 1 - (1 - e^{-T/2RC_1})^2 \approx 2e^{-T/2RC_1} \]

Usually \[ \varepsilon < 0.1\% \text{(cap. ratio error)} \] is acceptable.

\[ 2e^{-T/2RC} \leq 10^{-4} \]

\[ \Rightarrow \frac{RC_1}{T} = RC_1 f_c \leq \frac{1}{2\ln 20000} \approx 0.05 \]

or \[ RC_1 \leq \frac{T}{20} \left(= \frac{1}{20f_c} \right) \]

\[ f_c = 500\text{KHz}, \ C_1 = 5\text{pF, } R \leq 20K\Omega; \ f_c = 100\text{MHz, } C_1 = 2\text{pF, } R \leq 250\Omega \]

2. Clock Feedthrough Noise

* All switches directly connected to the integrating node generate clock feedthrough noises.

* All clock feedthrough noises are proportional to the sampling frequency. They may have a dc component.

* As soon as the clock feedthrough error voltage does not
saturate the OP AMP, it can be eliminated at the output by reconstruction filters (LPF).
* The dc component cause offset voltage problems.

3. Junction Leakage
* Worst-case (100°C or 125°C) leakage at the integrating node:
  \(~10\text{ nA/mil}^2\) \(5\mu\text{m} \times 5\mu\text{m}\) junction => 400 pA leakage
* \(f_{s, \text{max}}\) is about 25KHz in this case to avoid significant errors.
* The leakage cause dc offset voltages.

4. DC offset Voltage of the OP AMP

5. Finite Gain of the OP AMP.

\[
V_{out}(nT) = V_{c2}(nT) - \frac{1}{A_o} V_{out}(nT)
\]

\[
C_2[V_{c2}(nT) - V_{c2}(nT-T)] + C_1[V_{in}(nT) + \frac{1}{A_o} V_{out}(nT)] = 0
\]

\[
=> H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\left(\frac{C_1}{C_2}\right)\left[1 + \left(\frac{1 + C_1/C_2}{A_o}\right)\right]}{z - \left(1 + \frac{1}{A_o}\right)}/\left[1 + \left(\frac{1 + C_1/C_2}{A_o}\right)\right]
\]
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CHUNG-YU WU

\[
H(e^{j\omega T}) = H_z(e^{j\omega T}) = \frac{1}{1 + \left(\frac{1}{A_o}\right)(1 + C_1/2C_2) - j(C_1/C_2)/2A_o \tan(\omega T/2)}
\]

\[
H_z(z) = \frac{(C_1/C_2)}{z - 1}
\]

\[
F(\omega) = \frac{1}{1 - m(\omega) + j\theta(\omega)}
\]

\[
m(\omega) = -\frac{1}{A_o}(1 + \frac{C_1}{2C_2})
\]

\[
\theta(\omega) = \frac{C_1/C_2}{2A_o \tan(\omega T/2)}
\]

\[
\frac{1}{\sqrt{(1 - m)^2 + \theta^2}} \approx \frac{1}{1 - m} \approx 1 + m \quad \text{relative magnitude error}
\]

\[
\angle F(\omega) = \tan^{-1}\frac{-\theta}{1 - m} \approx \tan^{-1}\theta \quad \text{relative phase error}
\]

\[
\omega T \ll 1, \quad A_o > 1000, \quad C_1/C_2 \text{ normal value.}
\]

\[
A_o \omega T \gg 1 \quad \text{Ao>1000=>0.1%}
\]

\[
\omega >> \frac{1}{A_o T} = \frac{f_s}{A_o} \quad \text{Ao>100=>1%}
\]

\[
=> m \text{ and } \theta \text{ are very small. } \quad \text{<0.1%}
\]

But for \(\omega < 2/A_o T\), \(\theta\) is large.

6. Finite Bandwidth of the OP AMP.

\[
A(s) = \frac{-1}{1/A_o + S/\omega_o} \quad \text{single-pole response}
\]

Similarly

\[
m(\omega) = -e^{k_1}[1-K\cos\omega T]
\]

\[
k = \frac{C_2}{C_1 + C_2}
\]

\[
\theta(\omega) = -e^{k_1}K\sin\omega T
\]

\[
k_1 \equiv K\omega_o T/2
\]

If \(\omega_o T/2 = \pi \omega_o / \omega_c \gg 1 \Rightarrow m \rightarrow 0, \theta \rightarrow 0.
\]

**\(\omega_o \approx 5\omega_c\) is adequate.

* The unity-gain bandwidth \(\omega_o\) of the OP AMP should be (at least) five times as large as the clock frequency \(\omega_c\).
ω₀ vs ω𝑐:

1. Given ω₀, ω𝑐 should be chosen low enough so that the OP AMPS have enough time to settle.
   But ω𝑐 should not be too low, or the noise aliasing effect becomes serious
   the antialiasing and smoothing filters must be too selective and too complex.

2. Given ω𝑐, ω₀ should be just high enough to assure that the stage can settle within each clock phase. Any higher value worsens unnecessarily the noise aliasing effect, and raises the dc power and chip area requirements of the op-amps.

3. 
   \[ A₀ = 1000 \text{ (60dB)}, f_o = 10\text{MHz, } f_{p1} = 10\text{KHz} \]
   choose \( f_c = 2\text{MHz, and } f < 40 \text{KHz} \)
   Typically \( f/f_c \cong 48 \) i.e. \( \omega_o T \approx 1/4 \)

7. Finite Slew Rate of the OP AMP

   * The output voltage of the OP AMP must be settled down with the clock active duration.
     \( t_{\text{slew}} + t_{\text{settle}} < T_2 \)
   * May cause nonlinear distortion.

8. Nonzero OP AMP Output Resistance

   \[ 2R_o \left( \frac{C_1C_2}{C_1 + C_2} + C_L \right) \cong T_1 < \frac{1}{7} T_{\Phi_{2=1}} \]

   \( C_2 \): feedback cap; \( C_1 \): input cap; \( C_L \): load cap.

9. Overall considerations:

   For an integrator settling error of 0.1% or less, we must have

   \[ A_o \geq 5000 \]
   \[ \omega_o/\omega_c \geq 4 \]
   \[ T/R_{\text{on}}C_1 \geq 40 \]

10. Noise Generated in SC Circuits

    (1) Clock feedthrough noise

    (2) Noise coupled directly or capacitive from the power, clock, ground lines, and from the substrate.
(3) Thermal and flicker ($\frac{1}{f}$) noise generated in the switches and op-amps.

Thermal and flicker ($\frac{1}{f}$) noise:

* Internal sampling and holding => If $\frac{1}{f}$ noise has no aliasing => It can be eliminated.
* Thermal noise will be sampled and held with the OP AMP as a frequency limiting element. => $\omega_o >> \omega_c$ is not suitable.
* The circuit noise ↓ if the circuit cap. ↑
CH 15. Continuous-Time Filters in CMOS

§15-1 Categories of continuous-time filter ICs

<table>
<thead>
<tr>
<th>Amplifier Types</th>
<th>Continuous-Time Filter Types</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage OP AMP $A_V$</td>
<td>$O$ (Voltage-mode) Active RC filters</td>
</tr>
<tr>
<td>Current OP AMP $A_I$</td>
<td>$\Delta$ (Current-mode) Active RC filters</td>
</tr>
<tr>
<td>Finite-gain voltage amp</td>
<td>$\Delta$ (Voltage-mode) Active RC filters</td>
</tr>
<tr>
<td>Finite-gain current amp.</td>
<td>$\bullet$ (Current-mode) Active RC filters</td>
</tr>
<tr>
<td>Infinite-gain Operational Transconductance</td>
<td></td>
</tr>
<tr>
<td>Amp. (OTA) $G_m$</td>
<td>$\times$</td>
</tr>
<tr>
<td>Finite-gain OTA or $g_m$ amplifier</td>
<td>$O$ (Voltage-mode) $G_m$-C filters</td>
</tr>
<tr>
<td>Infinite-gain Operational Transimpedance</td>
<td></td>
</tr>
<tr>
<td>Amp. $R_m$</td>
<td>$\times$</td>
</tr>
<tr>
<td>Finite-gain Transimpedance Amp. or $R_m$</td>
<td>$\Delta$ (Current-mode) $R_m$-C filters</td>
</tr>
<tr>
<td>amplifier</td>
<td></td>
</tr>
<tr>
<td>Mixed $G_m$ and $R_m$ Amplifiers</td>
<td>$?$</td>
</tr>
<tr>
<td>Mixed $A_V$, $A_I$, $G_m$, and $R_m$ Amplifiers</td>
<td>$?$</td>
</tr>
<tr>
<td>RF amplifier</td>
<td>$\Delta$ Integrated LC filters</td>
</tr>
</tbody>
</table>

$O$ : well developed

$\Delta$ : less developed but with great potential

$\bullet$ : much less developed

$\times$ : not explored

$?$ : to be developed with potential

Common characteristics of continuous-time filters:

1. Not parasitic free
   
   $=>$ Greater tolerance in performance.

2. No switches or clocks
   
   $=>$ Lower noise (clock-induced) or simpler circuit.

3. Need tuning to accommodate the process variations on filter characteristics if high accuracy is required.
   
   $=>$ Extra overhead and higher cost.

   $=>$ Might not be needed if process-independent design is used and reasonable tolerance is allowed.
4. Could achieve higher-frequency operation in the VHF or UHF range if finite-gain amplifiers are used.
5. Could achieve GHz operation if deep submicron CMOS is used.

§15-2 Gm-C or OTA-C (Operational-Transconductance-Amplifier-C)

Filters

§15-2.1 Transconductor or OTA characteristics

Ideal characteristics:
\[ g_m = h_{IABC} \text{ or } h'V_{ABC} \]
\[ I_o = g_m(V^+ - V^-) \]
\[ R_i \to \infty, \quad R_o = 0 \]
\[ h(h') \] is a constant.

Nonideal characteristics:
\[ g_m \] is not linearly proportional to \( I_{ABC} \) or \( V_{ABC} \).
\[ R_i \] and \( R_o \) are finite.

§15-2.2 Basic OTA building blocks

1. Voltage amplifiers \( G_m \) or op amp + resistors.

(a) Basic inverting
\[ \frac{V_o}{V_i} = -g_m RL \]
\[ Z_o = RL \]

(b) Basic noninverting
\[ \frac{V_o}{V_i} = g_m RL \]
\[ Z_o = RL \]
(c) Feedback amplifier

\[ \frac{V_o}{V_i} = -\frac{g_m R_L}{1 + g_m R_1} \sim \frac{R_L}{R_1} \]

\[ Z_o = \frac{R_1 R_2}{1 + g_m R_1} \]

(d) Noninverting feedback amplifier

\[ \frac{V_o}{V_i} = -\frac{g_m R_L}{1 + g_m R_1} \sim +(1 + \frac{R_L}{R_1}) \]

\[ Z_o = \frac{R_1 R_2}{1 + g_m R_1} \]

(e) Buffered amplifier

(f) Buffered VCVC feedback

(g) All OTA amplifiers

\[ \frac{V_o}{V_i} = -\frac{g_{m1}}{g_{m2}} \]

\[ Z_o = -\frac{1}{g_{m2}} \]
2. Controlled impedance elements

(a) Single-ended voltage variable resistor (VVR)

(b) Floating VVR

(c) Scaled VVR

(d) Voltage variable impedance inverter

(e) Voltage variable floating impedance

(f) Impedance multiplier
(f) Super inductor

\[ Z\text{in} = \frac{s^2 C_1 C_2}{g_{m1} g_{m2} g_{m3}} \]

(f) FDNR

\[ Z\text{in} = \frac{g_{m1} g_{m2} g_{m3}}{s^2 C_1 C_2 g_{m1} g_{m2}} \]

(d) Variable Impedance Inverter (VIC) or Gyrator

* \( Z_L \) is a capacitor \( \Rightarrow \) \( Z_{\text{in}} \) is a inductor \( \Rightarrow \) active inductor.

* Can be used in voltage-controlled oscillator (VCO)

(h) FDNR (Frequency Dependent Negative Resistance)

\[ S = j\omega \quad Z_{\text{in}}(j\omega) = \frac{R}{\omega^2} \]

* Gyrator + super inductor.

3. Integrators \quad G_m \text{ or OTA + R or C}

(a) Simple

\[ \frac{V_o}{V_{i1} - V_{i2}} = \frac{g_m}{sC} \]

(b) Lossy

\[ \frac{V_o}{V_i} = \frac{g_m R}{sRC + 1} \]
§15-2.3 Gm-C or OTA-C filters (first-order)

(a) First-order lowpass voltage-controlled filter, fixed dc gain, pole adjustable

\[ H(s) = \frac{V_o}{V_i} = \frac{g_m}{sC + g_m} \]

(b) Lowpass, fixed pole, adjustable dc gain

\[ H(s) = \frac{V_o}{V_i} = \frac{g_m}{sC + \frac{1}{R}} \]

(c) Highpass, fixed high-frequency gain, adjustable pole

\[ H(s) = \frac{V_o}{V_i} = \frac{sc}{sC + g_m} \]
(d) Shelving equalizer, fixed high-frequency gain, fixed pole, adjustable zero

\[ H(S) = \frac{V_o}{V_i} = \frac{R(sC + g_m)}{sRC + 1} \]

(e) Shelving equalizer, fixed high-frequency gain, fixed zero, adjustable pole

\[ H(s) = \frac{V_o}{V_i} = \frac{g_m(1 + sRC)}{sc + g_m} \]

(f) Lowpass filter, adjustable pole and zero

\[ H(s) = \frac{V_o}{V_i} = \frac{sc_2 + g_m}{s(c_1 + c_2)g_m} \]

(g) Shelving equalizer, independently adjustable pole and zero

\[ H(s) = \frac{V_o}{V_i} = \frac{sC + g_{m1}}{sC + g_{m2}} \]
(h) Lowpass or highpass filter, adjustable zero and pole, fixed ratio or independent adjustment

\[ H(s) = \frac{g_m/(g_{m1}+g_{m2})}{s(C_1+C_2) + g_{m1} + g_{m2}} \]

(i) Phase shifter, adjustable with \( g_m \)

\[ H(s) = \frac{V_o}{V_i} = \frac{sC - g_{m1}}{sC + g_{m1}g_{m2}R} \]

\[ V_{01} = \frac{S^2C_1C_2V_C + SC_1g_{m2}V_B + g_{m1}g_{m2}V_A}{S^2C_1C_2 + SC_1g_{m2} + g_{m1}g_{m2}} \]
Transfer functions for the biquadratic structure (a)

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Input Conditions</th>
<th>Transfer Function</th>
<th>If $g_{m1}=g_{m2}=g_m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_0$ Adjustable Lowpass</td>
<td>$V_i=V_A$ $V_B$ and $V_C$ Grounded</td>
<td>$\frac{g_{m1}g_{m2}}{s^2C_1C_2 + SC_1g_{m2} + g_{m1}g_{m2}}$</td>
<td>$\frac{g_m}{\sqrt{C_1C_2}} \sqrt{\frac{C_2}{C_1}}$</td>
</tr>
<tr>
<td>$\omega_0$ Adjustable Bandpass</td>
<td>$V_i=V_B$ $V_A$ and $V_C$ Grounded</td>
<td>$\frac{sc_1g_{m2}}{s^2C_1C_2 + SC_1g_{m2} + g_{m1}g_{m2}}$</td>
<td>$\frac{g_m}{\sqrt{C_1C_2}} \sqrt{\frac{C_2}{C_1}}$</td>
</tr>
<tr>
<td>$\omega_0$ Adjustable Highpass</td>
<td>$V_i=V_C$ $V_A$ and $V_B$ Grounded</td>
<td>$\frac{s^2C_1C_2}{s^2C_1C_2 + SC_1g_{m2} + g_{m1}g_{m2}}$</td>
<td>$\frac{g_m}{\sqrt{C_1C_2}} \sqrt{\frac{C_2}{C_1}}$</td>
</tr>
<tr>
<td>$\omega_0$ Adjustable Notch</td>
<td>$V_i=V_A=V_C$ $V_B$ Grounded</td>
<td>$\frac{s^2C_1C_2 + g_{m1}g_{m2}}{s^2C_1C_2 + SC_1g_{m2} + g_{m1}g_{m2}}$</td>
<td>$\frac{g_m}{\sqrt{C_1C_2}} \sqrt{\frac{C_2}{C_1}}$</td>
</tr>
</tbody>
</table>

(b)

![Diagram](image)

* Can implement lowpass, bandpass, highpass, and notch.
* If $g_{m3}$ is fixed and $g_{m1}=g_{m2}=g_m$ is adjusted, the poles can be moved in a constant-$Q$ manner.
* If $g_{m3}$ is adjusted with $g_{m1}$ and $g_{m2}$ fixed, the pole movement in a constant-$\omega_0$ manner.

(c)

![Diagram](image)

$$V_{o3} = \frac{S^2C_1C_2V_A + SC_1g_{m2}V_B + g_{m2}g_{m1}V_A}{S^2C_1C_2 + Sg_{m3}C_1 + g_{m1}g_{m2}}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \ , \ Q = \frac{\sqrt{\frac{C_2g_{m1}}{C_1g_{m2}}}}{g_{m3}R}$$
* $\omega_o$ can be adjusted linearly with $g_{m1}=g_{m2}=g_m$ and $g_{m3}$ constant
  =>$\text{constant-bandwidth movement.}$
* If $g_{m1}$, $g_{m2}$, and $g_{m3}$ are adjusted simultaneously, constant-Q pole movement.
* Interchanging "$+$" and "-" terminals of $g_{m1}$ and $g_{m2}$ and setting $V_A=V_B=V_C=V_i$,
  and making $g_{m1}=g_{m2}=g_{m3}=g_m =>$ $2^{nd}$-order $g_m$ adjustable phase equalizer.

(d)

* The adjustment of the bandpass version with $g_{m1}=g_{m2}=g_m$ will result in a
  constant bandwidth, constant gain response.

(e) Elliptic biquadratic filter

* Can be applied to the realization of high-order voltage-controlled elliptic
  filters.
  =>$\text{Cascading these second-order blocks with interstage unity-gain buffers.}$
  =>$\text{All } g_m\text{'s are made equal and adjusted simultaneously.}$
* The voltage-controlled amplifier of Fig. (g) on p.15-3 can be
  inserted between $x$ and $x'$ The transconductance gain of the two OTAs in the
amplifier can be used as the control variable to adjust the ratio of the zero location to pole location.

(g) General biquadratic structure

\[
V_o = \frac{S^2C_1C_2V_A + SC_1g_mV_A + g_mg_AV_A}{S^2C_1C_2 + SC_1g_m + g_mg_A}
\]

* when \(V_i = V_A = V_B = V_C\), the \(\omega_o\) and Q for the poles and zeros can be adjusted by \(g_m\)'s to any desired value.

§15-2.5 Fully Differential Gm-C or OTA-C Filters

1. General first-order filter

\[
H(s) = \frac{V_{out}}{V_{in}} = \frac{K_1S + K_o}{S + \omega_o}
\]

\[
H(s) = \frac{SCx + G_{m1}}{S(C_A + C_X) + G_{m2}} = \frac{S(C_x) + G_{m1}}{C_A + C_x}
\]

\[
= C_x = (\frac{K_1}{1-K_1})C_A, \quad G_{m1} = K_0(C_A + C_X), \quad G_{m2} = \omega_0(C_A + C_X)
\]
2. General biquadratic filter

\[ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{K_2 S^2 + K_1 S + K_o}{S^2 + (\frac{\omega_o}{Q})S + \omega_o^2} \]

Design equations:

- \( C_X = \frac{C_B}{1 - K_2} \) where \( 0 \leq K_2 < 1 \)
- \( G_{m1} = \omega_o C_A \)
- \( G_{m2} = \omega_o (C_B + C_X) \)
- \( G_{m3} = \frac{\omega_o (C_B + C_X)}{Q} \)
- \( G_{m4} = (K_o C_A)/\omega_o \)
- \( G_{m5} = K_1 (C_B + C_X) \)
§15-3 CMOS Transconductor or OTA

1. CMOS transconductor using triode transistor

\[ G_m = \mu_n C_{ox} \frac{W}{L} (V_{gs9} - V_{in}) \]

* \( Q_9 \): operated in the triode region.
* \( G_m \) can be adjusted by \( V_{gs9} \) and scaled by the current mirrors \( Q_3/Q_7 \) and \( Q_4/Q_8 \).
* \( Q_5/Q_6 \) are feedback devices to set the drain voltages of \( Q_1/Q_2 \).

2. CMOS transconductor using varying bias-triode transistors.

\[ G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1 + 4k_3)} \]

* \( Q_3 \) and \( Q_4 \) are in the triode region.
* \( G_m = \frac{1}{r_d + \frac{r_{ds3} + r_{ds4}}{r_{ds3} || r_{ds4}}} \) where \( r_{ds3} = r_{ds4} = \frac{1}{2K_3(V_{GS1} - V_m)} \)
  \[ r_{s1} = r_{s2} = \frac{1}{g_m} = \frac{1}{2K_1(V_{GS1} - V_m)} \]
  \[ V_{GS1} - V_m = \sqrt{\frac{I_1}{K_i}} \]
3. CMOS differential-pair transconductor with floating voltage supply.
Conceptual circuit:

\[(i_{D1} - i_{D2}) = 4K_{eq}V_x(v_1 - v_2)\]

Real circuit:

\[(i_{D1} - i_{D2}) = 4\sqrt{K_{eq}I_B}(V_1 - V_2)\]

\[G_m = 4\sqrt{K_{eq}I_B}\]

* 30~50 dB linearity.

4. CMOS bias-offset cross-coupled transconductor.

\[(i_1 - i_2) = 2KV_B(V_1 - V_2)\]

\[G_m = 2KV_B\]

* 30~50 dB linearity
### §15-4 Design Example of Gm-C or OTA-C Filters


1. CMOS linear transconductance amplifier (CMOS inverter-based complementary differential-pair transconductor)

\[ g_m = 2k_{\text{eff}} (V_{G1} + |V_{G4}^\Sigma| - \Sigma V_T) \]

\[ \Sigma V_T = V_{Tn1} + V_{Tn3} + |V_{TP2}| + |V_{TP4}| \]

\[ k_{\text{eff}} = \frac{k_n k_p}{(\sqrt{|k_n|} + \sqrt{|k_p|})^2} \]

\[ k_{np} = \frac{1}{2} \left( \frac{u_{\text{eff}} c_{ox} \times W}{L} \right)_{n,p} \]

Tunable \( g_m \) amplifier symbol:

2. Gm-C biquad (general)

\[ H(s) = \frac{-C_1 g_m^2 S N_{BP} + C_1 g_m S^2 N_{LP} + g_m^2 N_{LP} + (C_1 C_2 g_m S^2 + g_m L g_m) N_{BR}}{C_1 C_2 g_m S^2 + C_1 g_m (g_m Q - g_m) S + g_m^3} \]

- **N\(B\)P**: \( V_B \neq 0, V_L = V_H = 0 \)
- **N\(H\)P**: \( V_H \neq 0, V_L = V_B = 0 \)
- **N\(L\)P**: \( V_L \neq 0, V_H = V_B = 0 \)
- **N\(B\)R**: \( V_L = V_H = V_{BR}, V_B = 0 \)
Experimental results on BP filter:

![Passband detail of the filter performance at 0°C (lower trace) and at 65°C.](image)

**Center frequency 4MHz**

**TABLE I**

<table>
<thead>
<tr>
<th>Control</th>
<th>Automatic</th>
<th>Manual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passband ripple</td>
<td>1 dB</td>
<td>0.5 dB</td>
</tr>
<tr>
<td>Stopband attenuation</td>
<td>&gt;60 dB</td>
<td></td>
</tr>
<tr>
<td>Bandwidth</td>
<td>800 KHz</td>
<td></td>
</tr>
<tr>
<td>S/N in passband</td>
<td>≈40dB</td>
<td>75dB</td>
</tr>
<tr>
<td>Distortion (for 0.5Vpp)</td>
<td>0.5%</td>
<td></td>
</tr>
<tr>
<td>Max. signal level</td>
<td>1.2 V_pp</td>
<td></td>
</tr>
<tr>
<td>Frequency control range</td>
<td>1 MHz</td>
<td>1.5 MHz</td>
</tr>
<tr>
<td>Q-control range</td>
<td>40%</td>
<td>unlimited</td>
</tr>
<tr>
<td>Offset (reference inverter)</td>
<td>1mV @ Gain ≈ 50</td>
<td></td>
</tr>
</tbody>
</table>

§15-5 MOSFET-C Filters

* MOSFET-C filters are slower than Gm-C filters
  · ′ Miller integration.
* Smaller speed
  · ′ The load of op amps is resistive
* Straightforward design methodology
1. Two-transistor integrators.

(a) Active-RC integrator

\[ R_1 = R_{p1} = R_{n1} \quad R_2 = R_{p2} = R_{n2} \]

\[ V_{\text{diff}} = V_{p0} - V_{n0} = \frac{i_{p1} - i_{n1} + i_{p2} - i_{n2}}{SC_1} \]

\[ = \frac{1}{SR_1C_1} (V_{p1} - V_{n1}) + \frac{1}{SR_2C_1} (V_{p2} - V_{n2}) \]

(b) Two-transistor MOSFET-C integrator

2. General biquadratic MOSFET-C filter

Active-RC circuit:

MOSFET-C biquadratic filter:
$$H(S) = \frac{V_o(s)}{V_i(s)} = \frac{\left(\frac{C_1}{C_B}\right)S^2 + \left(\frac{G_2}{C_B}\right)S + \frac{G_1G_3}{C_A C_B}}{S^2 + \left(\frac{G_1}{G_B}\right)S + \frac{G_3G_4}{C_A C_B}}$$

3. Four-transistor integrators

$$V_{diff} = V_{po} - V_{no}$$

$$\equiv \frac{1}{sr_{DS1}c_1} (V_{pi} - V_{mi}) + \frac{1}{sr_{DS2}c_1} (V_{mi} - V_{pi})$$

where $$r_{DS1} = \frac{1}{u_n c_{ox}(\frac{W}{L})(V_{c1} - V_x - V_t)}$$

$$r_{DS2} = \frac{1}{u_n c_{ox}(\frac{W}{L})(V_{c2} - V_x - V_t)}$$

All four transistors are matched

$$\Rightarrow V_{diff} = \frac{1}{sr_{DS}c_1} (V_{pi} - V_{mi})$$

where $$r_{DS} = \frac{1}{u_n c_{ox}(\frac{W}{L})(V_{c1} - V_{c2})}$$
CH 16. Oversampling Data Converters

§16-1 Fundamental Concept

§16-1.1 Oversampling without noise shaping

1. Quantization noise modeling

\[
x(n) \quad \triangleleft \quad \text{Quantizer} \quad \triangledown \quad y(n)
\]

\[e(n) = y(n) - x(n)\]

* \(e(n)\) can be approximated as an independent random variable uniformly distributed between \(\pm \frac{\Delta}{2}\) where \(\Delta\) is the difference between two adjacent quantization levels, i.e. \(V_{\text{LSB}}\).

* The quantization noise power \(P_e = \frac{\Delta^2}{12}\).

* The quantization noise power is independent of the sampling frequency \(f_s\).

* The spectral density of \(e(n)\), \(S_e(f)\) is white and all its power is within \(\pm \frac{f_s}{2}\).

\[
\int_{-f_s/2}^{f_s/2} S_e^2(f) df = \int_{-f_s/2}^{f_s/2} K_x^2 df = K_x^2 f_s = \frac{\Delta^2}{12}
\]

\[\Rightarrow K_x = \left(\frac{\Delta}{\sqrt{12}}\right) \frac{1}{f_s}\]

2. Oversampling Advantage

\[\text{Oversampling ratio } \text{OSR} = \frac{f}{2f_o}\]
Assume that the input signal is a sinusoidal wave between 0 and $\Delta 2^N$.

The signal power $P_s$ is

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}$$

With $H(f)$, $P_s$ remains the same since the signal's frequency content is below $f_o$, but the quantization noise power $P_e$ becomes

$$P_e = \frac{2 f_o \Delta^2}{f_s} = \frac{2 f_o \Delta^2}{12} = \frac{\Delta^2}{12} \left(\frac{1}{OSR}\right)$$

OSR $\times 2 \Rightarrow P_e \downarrow \frac{1}{2}$ or -3dB, or 0.5 bits

$$\text{SNR}_{\text{max}} = 10\log\left(\frac{P}{P_e}\right) = 10\log\left(\frac{3}{2} 2^{2N}\right) + 10\log(OSR)$$

$$= 6.02N + 1.76 + 10\log(OSR)$$

$\Rightarrow$ SNR enhancement obtained from oversampling: $10\log(OSR)$.  
SNR improvement of 3 dB/octave or 0.5 bits/octave

3. The advantage of 1-bit D/A converter
* Oversampling improves the SNR, but it does not improve linearity.
* Theoretically, 1-bit converter with $f_o=25$ KHz can obtain a 96-dB SNR(16 bits) if the sampling frequency $f_s=54,000$ GHz!
* The advantage of a 1-bit DAC is that it is inherently linear.

§16-1.2 Oversampling with noise shaping

1. The system architecture of a $\Delta\Sigma$ oversampling ADC is shown in the next page
Oversampling Delta-Sigma Analog-to-Digital Converters:

2. Noise-shaped ∆Σ modulator

Two independent inputs: \( U(z) \) and \( E(z) \)

Signal transfer function \( S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \)

Noise transfer function \( N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \)

\( \Rightarrow Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z) \)

If \( |H(z)| \to \infty \) for \( 0 < f < f_o \) \( \Rightarrow |S_{TF}(z)| \to 1 \) and \( |N_{TF}(z)| \to 0 \)

\( \Rightarrow \) Quantization noise ↓ and signal unchanged.

3. First-order noise shaping:
\[ H(z) = \frac{z^{-1}}{1 - z^{-1}} \] (Noninverting Forward-Euler SC integrator)

\[ S_{TF}(z) = \frac{H(z)}{1 + H(z)} = z^{-1} \]

\[ N_{TF}(z) = \frac{1}{1 + H(z)} = (1 - z^{-1}) \quad z = e^{j\omega T} = e^{j2\pi f_s} \]

\[ N_{TF}(f) = 1 - e^{-j2\pi f_s} = \sin\left(\frac{\pi f}{f_s}\right) \times (2j) \times (e^{-j\pi f_s f_s}) \]

\[ |N_{TF}(f)| = 2\sin\left(\frac{\pi f}{f_s}\right) \]

The quantization power noise power over 0 to \( f_o \) is

\[ P_e = \int_{-f_o}^{f_o} S_e^2(f) |N_{TF}(f)|^2 df = \int_{-f_o}^{f_o} \left(\frac{\Delta^2}{12}\right) \frac{1}{f_s} \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \]

Since \( f_o << f_s \), i.e. OSR>>1, \( \sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s} \)

\[ P_e \approx \left(\frac{\Delta^2}{12}\right) \left(\frac{\pi^2}{3}\right) \left(\frac{2f}{f_s}\right)^3 = \frac{\Delta^2 \pi^2}{36} \left(\frac{1}{OSR}\right)^3 \]

\[ P_s = \frac{\Delta^2 2^{2N}}{8} \Rightarrow \text{SNR}_{\text{max}} = 10 \log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2} 2^{2N}\right) + 10\log\left[\frac{3}{\pi^2} (OSR)^3\right] \]

\[ \Rightarrow \text{SNR}_{\text{max}} = 6.02N + 1.76 - 5.17 + 30 \log(\text{OSR}) \]

Double OSR \( \Rightarrow \text{SNR}_{\text{max}} \uparrow \) by 9dB or 1.5bits/octave

Without noise shaping: \( \text{SNR}_{\text{max}} \uparrow \) by 3dB/ octave or 0.5bits/ octave.

\[ Y = Z^{-1}U + E(1-Z^{-1}) \]

Block diagram:
SC implementation:

Can be eliminated by connecting the node A Directly to the node A'.

First-order noise shaping with 2-bit ADC and 2-bit DAC
4. Second-order noise shaping

\[ S_{TF}(Z) = Z^{-1} \]

\[ N_{TF}(Z) = (1 - Z^{-1})^2 \]

\[ Y = Z^{-1}U + (1 - Z^{-1})^2E \]

\[ |N_{TF}(f)| = [2 \sin(\frac{\pi f}{f_s})]^2 \]

\[ \Rightarrow P_e \approx \frac{\Delta \pi^4}{60} \left( \frac{1}{OSR} \right)^5 \]

\[ \text{SNR}_{\text{max}} = 10\log\left( \frac{P_{\Delta}}{P_e} \right) = 10\log\left( \frac{\frac{3}{2} 2^k}{\pi^4} \right) + 10\log\left( \frac{5}{\pi^4} \right) + 10\log(\text{OSR})^5 \]

\[ = 6.02N + 1.76 - 12.9 + 50\log(\text{OSR}) \]

\[ \text{OSR} \times 2 \Rightarrow \text{SNR}_{\text{max}} \uparrow \text{by 15dB/Octave or 2.5 bits/Octave} \]

General formula of \( \text{SNR}_{\text{max}} \) with \( k \)-order noise shaping:

\[ \text{SNR}_{\text{max}} = 6.02N + 1.76 - 10\log\left( \frac{2k + 1}{\pi^4} \right) + (2k + 1) 10\log(\text{OSR}) \]

\[ \text{OSR} \times 2 \Rightarrow \text{SNR}_{\text{max}} \uparrow \text{by 3}(2k+1)\text{dB/Octave or 0.5}(2k+1)\text{bits/Octave} \]

Noise-shaping transfer functions:

The SC implementation of the second-order \( \Delta\Sigma \) modulator is shown in the next page.

* Single-ended structure
* Can be converted into fully differential structure for better noise rejection and
linearity.
* The capacitor and switches in the feedback path to OP₂ can be reduced as shown on page 16-5.

SC implementation: Single-Ended type circuit diagram
§16-2 System Architecture of Oversampling ΔΣ ADC

1. Architecture

\[ X_{in}(t) \xrightarrow{\text{Anti-aliasing filter}} X_c(t) \xrightarrow{\text{Sample-and-hold}} X_{sh}(t) \xrightarrow{\Delta \Sigma \text{ Mod.}} X_{dom}(n) \xrightarrow{\text{Digital low-pass filter}} X_p(n) \xrightarrow{\text{Decimation filter}} X_s(n) \]

2. Signals and spectra

- \( X_c(t) \): Analog signal
- \( X_{sh}(t) \): Sampled signal
- \( X_{dom}(n) \): Digital signal
- \( X_p(n) \): Filtered signal
- \( X_s(n) \): Decimated signal

* The decimation process does not result in any loss of information, since the bandwidth of the original signal was assumed to be \( f_0 \). The spectral information is spread over \( 0 \sim \frac{\pi}{6} \) in \( X_{ep} \) and \( 0 \sim \pi \) in \( X_s \).
§16-3 System Architecture of Oversampling $\Delta\Sigma$ DAC

1. Architecture

\[ X_s(n) \xrightarrow{\text{OSR}} X_{s2}(n) \xrightarrow{\text{Interpolation (low-paa)}} X_{lp}(n) \xrightarrow{\Delta\Sigma} X_{dem}(n) \xrightarrow{\text{1-bit}} X_{da}(t) \xrightarrow{\text{Analog low-pass filter}} X_c(t) \]

\[ OSR = \frac{f_s}{2f_0} \]

2. Signals and spectra
§16-4 High-Order Modulators

Multi-stAge noise SHaping (MASH) architecture:
To use a cascade-type structure where the overall higher-order modulator is constructed using lower-order ones.
=> The stability could be maintained.

\[ Y = U z^{-1} + Q_1 (1 - z^{-1}) \]

\[ YZ^{-1} = Q_1 Z^{-1} + Q (1 - Z^{-1}) \]

\[ Y = U z^{-1} - Q (1 - Z^{-1})^2 \]

§16-5 Design Considerations

§16-5.1 Limitations on accuracy and linearity

A. Noise
- Thermal noise in resistors, conducing switches, op-amps. Usually aliased by sampling
- 1/f op-amp noise, dc offset
- Supply, ground and substrate noise
- clock feedthrough noise
- clock jitter noise
- quantization noise leakage
B. Nonlinear effects

- **R&C nonlinearities**
- **Amplifier nonlinearities**
- **Finite op-amp slew rate**
- **Signal-dependent clock feedthrough noise**
- **Signal-dependent sampling aperture noise**
- **Internal A/D and D/A nonlinearities**

**Linearity of 1-bit DAC:**

1. The two output levels somehow become functions of the low-frequency signals => Linearity limitation
   - Power supply voltage are changed for different low-frequency signals to cause distortion.
     => must be well-regulated.
   - The clock feedthrough of the input switches is also dependent on the gate voltage and thus the supply voltage.
     => low-frequency input signal dependent
   - The clock jitter could be a function of the low-frequency input signals.

2. The memory between output levels also causes severe linearity limitation.

![Diagram showing Ideal and Typical output levels]

<table>
<thead>
<tr>
<th>Binary Area for symbol</th>
<th>$A_i^{-\delta_1}$</th>
<th>$A_i$</th>
<th>$A_0^{-\delta_2}$</th>
<th>$A_0$</th>
<th>$A_i^{+\delta_1}$</th>
<th>$A_0^{+\delta_2}$</th>
<th>$A_i^{+\delta_1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta_1, \delta_2$: The area difference of the present binary state with different past states.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1→1: $\delta_1$</td>
<td>$1 \rightarrow -1$: $\delta_2$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average 0: 1, -1, 1, -1, -1, -1</td>
<td>$\overline{V_a(t)} = \frac{A_i + A_0}{2} + \frac{\delta_1 + \delta_2}{2}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average $\frac{1}{3}$: 1, 1, -1, 1, -1</td>
<td>$\overline{V_b(t)} = \frac{2A_i + A_0}{3} + \frac{\delta_1 + \delta_2}{3}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average $-\frac{1}{3}$: -1, -1, 1, -1, 1</td>
<td>$\overline{V_c(t)} = \frac{A_i + 2A_0}{3} + \frac{\delta_1 + \delta_2}{3}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Ideal case: $\delta_1 = \delta_2 = 0$, practical case: $\delta_1 \neq \delta_2 \neq 0$

=>$\text{Three averages do not lie on a straight line}=>$Nonlinear.

How to improve this nonlinearity?
1. $\delta_1 = -\delta_2$ : To match falling and rising signals =>$\text{Very difficult to achieve.}$
2. The use of memoryless coding scheme, i.e. return-to-zero (RTZ) coding scheme.

<table>
<thead>
<tr>
<th>Binary</th>
<th>1</th>
<th>1</th>
<th>-1</th>
<th>-1</th>
<th>1</th>
<th>-1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>$A_1$</td>
<td>$A_1$</td>
<td>$A_0$</td>
<td>$A_0$</td>
<td>$A_1$</td>
<td>$A_0$</td>
<td>$A_1$</td>
</tr>
</tbody>
</table>

$1 : -1 \rightarrow 1 \text{ and } 1 \rightarrow 1$ Every 1 has the same area.
$-1 : -1 \rightarrow -1$ Every -1 has the same area.

=>$\text{Better linearity.}$

3. Basically, SCF or SC circuits are memoryless if enough time is left for settling on each clock phase.

Idle tones phenomena
1-bit DAC

dc level $\frac{1}{3}$ =>$y(n)=\{1, 1, -1, 1, 1, -1, \ldots\}$ periodic pattern with the power concentrated at dc and $\frac{f_s}{3}$.

After low-pass filter =>$\text{only dc level remains.}$

dc level $\frac{1}{3} + \frac{1}{24} = \frac{3}{8}$ =>$y(n)=\{1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, \ldots\}$
periodic pattern with 16 cycles and some power at dc and $\frac{f_s}{16}$.

$=>$ lowpass filter

$=>$ dc level $\frac{3}{8}$ and $\frac{f_s}{16}$ tone

(∵ $f_0 = \frac{f_s}{16}$ is assumed and lowpass filter will not attenuate $f_s/16$ signal)

$=>$ Low-frequency tones cannot be filtered out by the lowpass filter and can lead to annoying tones in the audible range. They exist even in high-order modulators. There tones might be a signal varying over some frequency range in a random-like fashion.

Dithering technique to reduce idle tones.

- To add the dithering signal to the modulator just before its quantizer.
- The dithering signal has a white-noise type spectrum and is a random (pseudo-random) signal.
- The dithering signal breaks up the tones so that they never occur.
- Add about 3-dB extra in-band noise
- Require rechecking the modulator's stability.

§16-6 Advantages and Applications

Advantages of Delta-Sigma Converters:
- Low-Complexity Analog, High-Complexity Digital
- High-Resolution Conversion
- Low-Precision Analog (no trimming)
- Simple Anti-Aliasing Filters
- No Sample & Hold Needed
- Can be Built Completely In CMOS
- Overall Small Chip Area in Fine-Line Technology
- Can be Integrated on Chip With Other DSP Functions
- Ideally Suit for Rates up to and Including Audio Band

Commercial Applications Well-Suited for Delta-Sigma ADC
- Standard Voice Band Telephony
  13-bit dynamic range, 8-bit linearity (u/A-Law), 8KHz Sampling rate
- Digital Mobile Radio (same req. as above)
• High-Precision Voice-Band (CCITT V.32 9600-Baud Modems)
  14-15 bit dynamic range, 12-bit linearity, 3-4kHz BW, 9600 Sampling rate
• ISDN Wideband Speech (CCITT G.722)
  13-bit dynamic range, 16kHz Sampling rate
• ISDN U-Interface
  13-bit dynamic range, 80kHz Sampling rate, 160kb/s Transmission Rate
• Audio-Band (CD, DAT; stereo (2))
  16-18-bit (18-20 bit) resolution, 14-16 bit)(15-16bit) linearity, 48kHz Sampling Rate
• 5 1/2 Instrumentation A/D Converter
  20 bit resolution, 0.1-10Hz BW with Self-Calibration Circuit
• Integration with Digital Signal Processors
• Ideally Suited for Rates up to and Including Audio Band

A variety of applications from voice-band through audio-band

§16-7 Examples

2\textsuperscript{nd}-order ΔΣ modulator implemented by fully differential SC circuit.
Testing Environment:

Digital-to-Analog Converter

Precision Function Generator

Pure test Pattern

Low-noise cable

Good Transmission Line

ΔΣ ADC

Measurement

Chip under test

*Develop design-for-testability ADC and environment

The measured SNR versus input signal level.

SNR

SIN Ratio (dB)

-100 -80 -60 -40 -20 0 20

Input Signal Level (dB)

Sampling rate 2048KHz
Input signal 8KHz
Time record comprises 16384 points
20KHz notional baseband
1. Applications of PLLs:
1. Clock recovery in communication and digital systems.
2. Frequency synthesizer used in televisions or wireless communication systems to select different channels.
3. Demodulation of FM signals.

2. Basic PLL architecture:

If the phase detector is of analog-multiplier type, its output voltage $V_{pd}$ can be written as

$$V_{pd} = K_M V_{in} V_{osc} = K_M E_{in} E_{osc} \sin(\omega t) \cos(\omega t - \phi_d)$$

where $\phi_d$ is the phase difference between the input signal $V_{in}$ and the output $V_{osc}$ of the VCO.

Since the lowpass filter is to remove the high-frequency ($2\omega$) term, the signal $V_{cntl}$ is given by

$$V_{cntl} = K_{lp} K_M \frac{E_{in} E_{osc}}{2} \sin(\phi_d)$$

$$\approx K_{lp} K_M \frac{E_{in} E_{osc}}{2} \phi_d = K_{lp} K_{pd} \phi_d$$

where $K_{pd} = K_M \frac{E_{in} E_{osc}}{2}$

The frequency of VCO can be expressed as

$$\omega_{osc} = K_{osc} V_{cntl} + \omega_{fr}$$

where $\omega_{fr}$ is the free-running frequency of the VCO with its control voltage $V_{cntl} = 0$.

$$\Rightarrow V_{cntl} = \frac{\omega_{in} - \omega_{fr}}{K_{osc}}$$
where $\omega_{in}$ is the frequency of the input signal, which is equal to the frequency of VCO output when the PLL is in the locked state.

$$\Rightarrow \phi_d = \frac{V_{cntl}}{K_{lp}K_{pd}} = \frac{\omega_{in} - \omega_{fr}}{K_{lp}K_{pd}K_{osc}}$$

3. Linearized small-signal analysis

When a PLL is in lock, its dynamic response to input-signal phase and frequency changes can be well approximated by a linear model, as long as these changes are slow and small about their operating point.

A signal-flow graph for the linearized small-signal model of a PLL when in lock:

$$V_{cntl}(s) = K_{pd}K_{lp}H_{lp}(s)[\phi_{in}(s) - \phi_{osc}(s)]$$

$$\phi_{osc}(s) = K_{osc}(V_{cntl}(s)/s) \quad (\because \omega(t) = \frac{d\phi(t)}{dt}, \quad \phi(s) = \frac{\omega(s)}{s})$$

$$\Rightarrow \frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{SK_{pd}K_{lp}H_{lp}(s)}{S + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

* General transfer function applicable to almost every PLL.
* Different PLLs $\Rightarrow$ Different $H_{lp}(s)$, $K_{pd}$, $K_{osc}$.

If a lead-lag lowpass filter is used in $H_{lp}(s)$, we have

$$H_{lp}(s) = \frac{1 + s\tau_z}{1 + s\tau_p} \quad \tau_z << \tau_p$$

$$\Rightarrow H(s) = \frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{1}{K_{osc}} S(1 + s\tau_z)$$

$$1 + S\left(\frac{1}{K_{pd}K_{lp}K_{osc}} + \tau_z\right) + \frac{s^2\tau_p}{K_{pd}K_{lp}K_{osc}}$$

* $H(s) = 0$ as $s \rightarrow 0 \Rightarrow \Delta \phi_{in} = 0$ leads to $\Delta V_{cntl} = 0$
\[ \frac{V_{out}(s)}{\omega_{in}(s)} = \frac{1}{K_{osc}} S(1 + s \tau_z) \]

\[ 1 + S\left(\frac{1}{K_{pd}K_{lp}K_{osc}} + \tau_z \right) + \frac{s^2 \tau_p}{K_{pd}K_{lp}K_{osc}} \]

\[ * \frac{V_{out}(s)}{\omega_{in}(s)} \bigg|_{s=0} = \frac{1}{K_{osc}} \]

The above second-order s-domain transfer functions have \( \omega_o \) and \( Q \) as

\[ \omega_o = \sqrt{\frac{K_{pd}K_{lp}K_{osc}}{\tau_p}} = \frac{K_{pll}}{\sqrt{\tau_p}} \]

\[ Q = \frac{1}{\sqrt{\frac{K_{pd}K_{lp}K_{osc}}{\tau_p} + \tau_z \sqrt{K_{pd}K_{lp}K_{osc}}}} = \frac{1}{1 + \frac{\tau_z K_{pll}}{\tau_p}} \]

* \( Q = \frac{1}{2} \rightarrow \) good settling behavior

\( Q = \frac{1}{\sqrt{3}} = 0.577 \rightarrow \) maximally flat group delay

\( Q = \frac{1}{\sqrt{2}} = 0.707 \rightarrow \) maximally flat amplitude response

* Usually \( Q = \frac{1}{2} \) is recommended in PLLs

In most cases, when \( \omega_o \ll \omega_{fr} \), we have

\[ \tau_z \gg \frac{1}{K_{pll}^2} \]

\[ \Rightarrow Q \approx \frac{\sqrt{\tau_p}}{\tau_z K_{PLL}} = \frac{1}{\omega_o \tau_z} = \frac{1}{2} \]

\[ \Rightarrow \tau_z = \frac{2 \sqrt{\tau_p}}{K_{PLL} \omega_o} = \frac{2}{\omega_o} \]

The transient time constant \( \tau_{PLL} \) of the complete loop for small phase or frequency changes can be expressed as

\[ \tau_{PLL} \approx \frac{1}{\omega_o} \]
Design considerations:  
1. Choosing $K_{pd}$ and $K_{osc}$ based on practical considerations  
2. Choose $\tau_p$ to achieve the desired loop settling time  
3. Choose $\tau_Z$ to obtain the desired $Q$ of the loop

If $\tau_Z = 0$, $\Rightarrow Q = \sqrt{\tau_p} K_{pll}$,  
$$\omega_o = \frac{K_{pll}^2}{Q} = \frac{K_{pd}K_{osc}}{Q} \quad (K_{lp} = 1)$$

4. Capture range and acquisition time  
Capture range: The maximum difference between the input signals' frequency and the VCO free-running frequency where lock can eventually be attained.  
The capture range is on the order of the pole frequency of the lowpass filter.  
Acquisition time: The time required to attain lock If the initial difference between the input signal's frequency and the VCO frequency is moderately large, the acquisition time $t_{acq}$ is  
$$t_{acq} \cong \frac{Q(\omega_{in} - \omega_{osc})^2}{\omega_o^3}$$

* If a PLL is designed to have a narrow loop bandwidth $\omega_o$, $t_{acq}$ can be quite large and lock is attained too slowly.  
Solution: 1. To add a frequency detector that detect when $\omega_{in} - \omega_{osc}$ is large. Then drive the loop toward lock much more quickly. When $\omega_{in} - \omega_{osc}$ is small, the frequency detector and the driver are disabled.  
2. To design the lowpass filter with a programmable pole frequency $\omega_o$.  
   Initial acquisition: $\omega_o \uparrow$ speed up acquisition.  
   Lock : $\omega_o \downarrow$ increase noise rejection.  
3. To sweep the VCO's frequency range during acquisition with the PLL disabled. When $\omega_{osc} \rightarrow \omega_{in}$, sweeping is disabled and PLL is activated.

5. Lock range  
Lock range: Once lock is attained, the PLL remains in lock over a range as long as the input signal's frequency $\omega_{in}$ changes only slowly. This range is the lock range, which is much larger than the capture range.  
$$V_{cntl-max} = K_{lp} K_M \frac{E_{in} E_{osc}}{2} = K_{lp} K_{pd}$$  
$$\Rightarrow \omega_{lock} = \pm K_{osc} K_{lp} K_{pd}$$
§17-2 Phase Detectors in PLLs

Three categories: 1. Analog phase detectors (PDs) or multipliers:
   Rely on the DC component when multiplying two sinusoidal waveforms of the same frequency.

2. Sequential circuits (e.g. EXOR and Flip-Flop PDs):
   Operate on the information contained in the zero-crossings of the input signal to aid acquisition when the loop is out of lock.

3. Phase-frequency detector:
   Provide a frequency sensitive signal to aid acquisition when the loop is out of lock. Also a sequential circuit actually.

§17-2.1 Multiplier PD

\[ V_{pd} = K_M E_{in} E_{osc} \sin(\omega_1 t + \theta_1) \cos(\omega_2 t + \theta_2) \]
\[ = K_M \frac{E_{in} E_{osc}}{2} \{ \sin((\omega_1 - \omega_2)t + \theta_1 - \theta_2) + \sin((\omega_1 + \omega_2)t + \theta_1 + \theta_2) \} \]

At phase lock, \( \omega_1 = \omega_2 \)

\[ \Rightarrow V_{pd} = K_M \frac{E_{in} E_{osc}}{2} [\sin(\theta_1 - \theta_2) + \sin(2\omega t + \theta_1 + \theta_2)] \]

After the lowpass filter, we have

\[ V_{pd} = K_{lp} K_M \frac{E_{in} E_{osc}}{2} \sin(\theta_1 - \theta_2) = K_M \frac{E_{in} E_{osc}}{2} \sin \theta_d \propto \theta_d \text{ if } \theta_d \text{ is small.} \]

* The multiplier PD is especially useful in applications where the reference frequency is too high and where the loop bandwidth is sufficiently narrow so that the filtering of the undesired components can be effective.

* The loop could lock to harmonics of the input signal.
  \( \Rightarrow \text{False lock} \)

* \( \omega_1 = \omega_2 \) is required.

§17-2.2 EXOR PD

![EXOR diagram](attachment:image.png)
* when \( A(V_{\text{in}}) \) and \( B(V_{\text{osc}}) \) are \( 90^\circ \) out of phase, the output \( V_{pd}(c) \) has \( \omega=2\omega_{\text{in}} \) and 50% duty cycle. This is a reference point. \( V_{pd} \propto \theta_d \) for \( 0^\circ<\theta_d<180^\circ \).

* False lock could occur
* \( \omega_1=\omega_2 \) is required.

§17-2.3 Flip-Flop PD

* The average value of \( V_{pd} \) or \( C \) has the shape of a saw tooth, with a linear range of a full cycle.

* At the center of the linear range of \( V_{pd} \) average, the most important harmonic is situated at the fundamental of the reference frequency as compared to the twice of reference frequency in the EXOR PD.
§17-2.4 Charge-pump PD

1. Desirable features:
   1. It does not exhibit false lock.
   2. $V_{in}$ and $V_{osc}$ are exactly in phase when the loops in lock.
   3. The PLL attains lock quickly even when $\omega_{in}$ is quite different from $\omega_{fr}$. 
Some typical waveforms of a charge-pump PD

\[
\begin{align*}
V_{in} & \uparrow \quad (\text{level}) \\
V_{osc} & \uparrow \quad (\text{level}) \\
\Delta \phi_{in} & \quad (\text{angle}) \\
2\pi & \quad (\text{time unit}) \\
2. \text{Small-signal analysis of a charge-pump PLL:} \\
\text{The average charge flow into the lowpass filter is} \\
I_{avg} &= \frac{\Delta \phi_{in}}{2\pi} I_{ch} \\
I_{avg} &= K_{pd}(\phi_{in} - \phi_{osc}) = K_{pd}\Delta \phi_{in} \\
\Rightarrow K_{pd} &= \frac{I_{ch}}{2\pi} \\
\text{For the lowpass filter } R, C_1 \text{ has a transfer function } H_{lp}(s) \text{ as} \\
H_{lp}(s) &= \frac{V_{in}(s)}{I_{avg}(s)} = R + \frac{1}{SC_1} = \frac{1 + SRC_1}{SC_1} \\
\text{Substituting } H_{lp}(s) \text{ and } K_{pd} \text{ into the transfer function } \\
\frac{V_p(s)}{\phi_{in}(s)}, \\
\text{we have} \\
\frac{V_p(s)}{\phi_{in}(s)} &= \frac{1}{K_{osc}} \cdot \frac{S(1 + SRC_1)}{1 + SRC_1 + \frac{S^2C_1}{K_{pd}K_{osc}}} \\
\Rightarrow \omega_o &= \sqrt{\frac{K_{pd}K_{osc}}{C_1}} \\
Q &= \frac{1}{RC_1 \omega_o} = \frac{1}{R \sqrt{C_1 K_{pd} K_{osc}}} = \frac{1}{R \sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}}}
\end{align*}
\]
3. Design Considerations:
(1) Choose $I_{ch}$ based on practical consideration like power dissipation and speed.
(2) $\omega_0$ is chosen according to the desired transient settling-time constant $\tau_{PLL}$ as
$$\omega_0 = \frac{1}{\tau_{PLL}}$$
(3) $C_1$ is chosen from the equation of $\omega_0$ whereas $R$ is chosen using the equation of $Q$.
The chosen $Q$ value is slightly less than what is eventually desired. $R \uparrow \Rightarrow Q \downarrow$
(4) Add $C_2$ to minimize glitches.
$C_2 \Rightarrow Q \uparrow \Rightarrow$ chosen $Q$ value is smaller $\Rightarrow$ Exact $Q$.
$$C_2 \geq \frac{1}{8} \sim \frac{1}{10} \text{ of } C_1$$
$$\Rightarrow H_{lp}(s) = \frac{R}{1 + SRC_2} + \frac{1}{SC_1}$$

4. Phase/Frequency detector (PFD)
* The most common sequential phase detector is the PFD.
* Asynchronous sequential logic circuit.
* 4 NOR-type RS flip-flops.
* Can also be realized in NAND gates.

![Phase/Frequency Detector Diagram](attachment:image.png)

* Basic operating principle:
Assume the PLL is in lock with $V_{in}$ leading $V_{osc}$
Initial conditions: $P_u=0$, $P_d=0$, $P_{u-dsbl}=0$, $P_{d-dsbl}=0$, $Reset=0$, $V_{in}=0$, $V_{osc}=0$
inputs: 1001
\( V_{\text{in}} \rightarrow 1 \) => \( P_u = 1 \) => Charge pumping starts and \( V_{\text{lp}} \uparrow \Rightarrow \omega_{\text{osc}} \uparrow \\
\( V_{\text{osc}} \rightarrow 1 \) => Reset nor gate inputs: 0001\( \rightarrow \)0000 \( \Rightarrow \) Reset 0\( \rightarrow \)1  \\
\( \Rightarrow \) \( P_u = 0 \) and \( P_d = 0 \) after one gate-delay ; \( P_d 0\rightarrow 1 \rightarrow 0 \)  \\
\( \Rightarrow \) \( P_{u-dsbl}=1 \) and \( P_{d-dsbl}=1 \) after two gate-delays.  \\
\( \Rightarrow \) Reset 1\( \rightarrow \)0 after one gate-delay of \( P_{u-dsbl}\rightarrow 1 \) and \( P_{d-dsbl}\rightarrow 1 \) or after three gate-delays of \( V_{\text{osc}} \rightarrow 1 \).  \\
\( \Rightarrow \) Keeping \( P_u = 0 \) and \( P_d = 0 \) \( \Rightarrow \) No charge pumping. \\
It is only when \( V_{\text{in}} 1\rightarrow 0 \Rightarrow \) FF3 is reset and \( P_{u-dsbl}=0 \)  \\
\( V_{\text{osc}} 1\rightarrow 0 \Rightarrow \) FF4 is reset and \( P_{d-dsbl}=0 \)  \\

* The waveforms of a PFD when \( V_{\text{in}} \) is at a higher frequency than \( V_{\text{osc}} \).  \\
\( \omega_{\text{in}} > \omega_{\text{osc}} \Rightarrow P_u = 1 \Rightarrow \) Charge pumping to increase \( \omega_{\text{osc}} \) until lock is achieved.  \\

* Transfer characteristic of a charge-pumping PFD
§17-3 Loop Filters and Loop Gains

§17-3.1 First-order PLL with zero-order loop filter

Loop gain of the feedback structure with \( \phi_{in}(s) \) and \( V_{cntl}(s) \)

\[
\text{Loop gain} = GH(s) = K_{pd} K_{lp} K_{osc} H_{lp}(s) \frac{1}{s}
\]

Zero-order loop filter: \( H_{lp}(s) = 1 \)

\[
\Rightarrow GH(S) = K_{pd} K_{lp} K_{osc} \frac{1}{s}
\]

PLL with zero-order loop filter

\[
\frac{V_{cntl}(s)}{\phi_{os}(s)} = \frac{SK_{pd} K_{lp}}{S + K_{pd} K_{lp} K_{osc}}
\]

Close-loop transfer function
§17-3.2 Second-order PLL with first-order loop-filter

First-order loop filter: \( H_{lp}(s) = \frac{1}{1 + S/\omega_p} \)

\[ \Rightarrow GH(s) = \frac{K_{pd} K_{lp} K_{osc}}{S(1 + S/\omega_p)} = \frac{\omega_p K_{pd} K_{lp} K_{osc}}{S^2 + \omega_p S} \]

PLL with first-order loop filter
\[ \Rightarrow \text{2nd-order type-1 PLL} \]

\[
\frac{V_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{S\omega_p K_{pd} K_{lp} K_{osc}}{S^2 + \omega_p S + \omega_p K_{pd} K_{lp} K_{osc}}
\]

§17-3.3 Third-order PLL with second-order loop filter

To improve the transient characteristics of the PLL, a low-frequency pole \( \omega_a \) is introduced in the loop filter. \( \Rightarrow \) Extra phase shift of 90°.

To compensate the extra phase shift, a compensating zero \( \omega_z \) must be introduced in order to keep the phase margin high enough.

2nd-order loop filter: \( H_{lp}(s) = \frac{1 + S/\omega_z}{(1 + S/\omega_p)(1 + S/\omega_a)} \)

\[ \Rightarrow GH(S) = \frac{K_{pd} K_{lp} K_{osc}(1 + S/\omega_z)}{S(1 + S/\omega_p)(1 + S/\omega_a)} \]

\[ \Rightarrow \text{Third-order type-1 PLL} \]

\[
\frac{V_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{S(1 + S/\omega_p)(1 + S/\omega_a) + K_{pd} K_{lp} K_{osc}(1 + S/\omega_z)}{S(1 + S/\omega_p)(1 + S/\omega_a)}
\]

If \( \omega_a = 0 \)
\[ \Rightarrow \text{Third-order type-2 PLL.} \]
§17-3.4 Third-order type-2 charge-pump PLL

\[ H_{lp}(s) = \frac{1 + s\tau_z}{s(C_z + C_p)[1 + s\tau_p]} \]

\[ \tau_z = R_z C_z \]
\[ \tau_p = R_z(C_z^{-1} + C_p^{-1})^{-1} \]

\[ \Rightarrow G_H(s) = \frac{K_{pd}K_{wp}K_{osc}(1 + s\tau_z)}{S^2(C_z + C_p)(1 + s\tau_p)} \]

§17-4 Voltage-Controlled Oscillators (VCOs)

Basic VCO specifications/requirements:
1. phase stability:
   The output spectrum of the VCO should approximate as good as possible the theoretical Dirac-impulse of a single sine wave, i.e. low phase noise.

   The definition of phase noise:
   \[ L(\Delta\omega) = 10 \log \left( \frac{\text{noise power in a 1-Hz bandwidth at freq. } \omega + \Delta\omega}{\text{carrier power}} \right) \text{ units: } \text{dBc/Hz} \]

2. Electrical tuning range
   The VCO must be able to cover the complete required frequency band of the application, including initial frequency offsets due to process variations.

3. Tuning linearity
   To simplify the design of the PLL, the VCO gain \( K_{osc} \) should be
constant.

4. Frequency pushing (MHz/V)
   The dependency of the center frequency on the power supply voltage.

5. Frequency pulling
   The dependence of the center frequency

6. Low cost

§17-4.1 Relaxation oscillator as VCO
* Multivibrator-based nonlinear oscillator.
* $f_{osc}$ in the order of a few 100 MHz
* In CMOS, phase noise value of -90dBc/Hz at 500KHz offset.

§17-4.2 Ring oscillator as VCO
* $T_{osc}=2n \cdot T_d$  n: number of inverters;  $T_d$: one inverter delay.
* Tuning: varying the current of the inverters.
* High phase noise: `switching action introduces a lot of disturbances.
* Power consumption ↑ linearly =>  phase noise ↓
* Typical phase noise:
  -94dBc/Hz at 1 MHz offset from a 2.2GHz carrier.
  -83dBc/Hz at 100 KHz offset from a 900MHz carrier.
* Circuit structure
  1. Three-stage ring oscillator
     ![Inverter Diagram]
  2. Differential two-stage ring oscillator
     ![Differential Inverter Diagram]
3. 1-stage-delay ring oscillator

\[ G_m \]

\[ f_{osc} \text{ MHz} \sim \text{GHz} \]


§17-4.3 \textit{LC-oscillator as VCO}

* Typically a 20dB better phase noise obtained over ring and relaxation oscillators.
* High-speed operation is possible due to the simple working principle.
* The realization of the inductor is the key point.

Design example: 0.7µm CMOS planar-LC VCO.
* Constant current => To limit power dissipation
* M₁ and M₂: To provide a negative resistance for oscillation
* \( L₁=L₂=3.2 \text{nH planar spiral inductors} \)
* \( p^+ – n \text{-well junction diodes } C₁ \) and \( C₂ \) as varactors for frequency tuning by \( V_c \).
  \( C₁=C₂ \approx 1 \text{pF} \)
* Different output voltage.

Chip photograph of the VCO. (Die size 750×750 µm²)

Measurement results:
1. Measured output spectrum for a carrier frequency of 1.81 GHz.
2. Measured phase noise w.r.t. frequency offset

![Graph showing phase noise vs. frequency offset]

Phase noise: -116dBc/Hz at 600 KHz offset

3. Measured frequency tuning characteristics

![Graph showing phase noise vs. frequency offset]

* At $V_c=0.5V$, the diode varactors $C_1$ and $C_2$ have a larger leakage current => Phase noise $\uparrow$ 3dB.
§17-4.4 Comparisons of Integrated VCOs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology [-]</th>
<th>Freq. [GHz]</th>
<th>Power [mW]</th>
<th>Tuning [%]</th>
<th>Phase noise [dBc/Hz] reported</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Relaxation oscillators</strong></td>
<td></td>
<td></td>
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<tr>
<td>[Banu JSSC88]</td>
<td>0.75-um CMOS</td>
<td>0.56</td>
<td>50</td>
<td>100</td>
<td>-90 @500kHz</td>
<td>Tuning from 100kHz to 1GHz</td>
</tr>
<tr>
<td>[Sneep JSSC90]</td>
<td>3-GHz Bip</td>
<td>0.1</td>
<td>30</td>
<td>100</td>
<td>-118 @1MHz</td>
<td>Tuning from low freq. to 150MHz</td>
</tr>
<tr>
<td>[Dobos CICC94]</td>
<td>9-GHz Bip</td>
<td>0.4</td>
<td>?</td>
<td>100</td>
<td>-110 @1MHz</td>
<td>Tuning from 800kHz to 800MHz; Fast start-up</td>
</tr>
<tr>
<td><strong>Ring oscillators</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Kwasn CICC95]</td>
<td>1.2-um CMOS</td>
<td>0.74</td>
<td>6.5</td>
<td>6</td>
<td>-89 @100kHz</td>
<td>Comparison of 3 designs</td>
</tr>
<tr>
<td>[Razav JSSC96]</td>
<td>0.5-um CMOS</td>
<td>2.2</td>
<td>NA</td>
<td>NA</td>
<td>-94 @1MHz</td>
<td>Three-stage; differential gain stage</td>
</tr>
<tr>
<td>[vd Tan ISSCC97]</td>
<td>9-GHz BiCMOS</td>
<td>2.0</td>
<td>NA</td>
<td>95</td>
<td>-106 @2MHz</td>
<td>Two-stage CCO; stacked with mixer</td>
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<tr>
<td><strong>LC-tuned oscillators</strong></td>
<td></td>
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<td></td>
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<tr>
<td>[Nguye JSSC92]</td>
<td>10-GHz Bip</td>
<td>1.8</td>
<td>70</td>
<td>10</td>
<td>-88 @100kHz</td>
<td>High-ohmic substrate; tuning with 2 tanks</td>
</tr>
<tr>
<td>[Based ESSC94]</td>
<td>1-um CMOS</td>
<td>1.0</td>
<td>16</td>
<td>0</td>
<td>-95 @100kHz</td>
<td>Wide metal turns; substrate back-etched</td>
</tr>
<tr>
<td>[Soyue JSSC96a]</td>
<td>12-GHz BiCMOS</td>
<td>2.4</td>
<td>50</td>
<td>0</td>
<td>-92 @100kHz</td>
<td>4-level, extra thick metal; high-ohmic substrate</td>
</tr>
<tr>
<td>[Ali ISSCC96]</td>
<td>25-GHz Bip</td>
<td>0.9</td>
<td>10</td>
<td>N.A.</td>
<td>-101 @100kHz</td>
<td>Complete PLL; planar inductors</td>
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</table>

*at 600 kHz offset from a 1.8-GHz carrier
<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology [-]</th>
<th>Freq. [GHz]</th>
<th>Power [mW]</th>
<th>Tuning [%]</th>
<th>Phase noise [dBc/Hz]</th>
<th>Remarks</th>
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<tr>
<td>LC-tuned oscillators(cont'd)</td>
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<tr>
<td>[Rofou ISSCC96]</td>
<td>1-um CMOS</td>
<td>0.9</td>
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<td>-85 @ 100kHz</td>
<td>-95 Front-etched inductors; quadrature signals</td>
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<td>[Soyue JSSC96b]</td>
<td>0.5-um BiCMOS</td>
<td>4.0</td>
<td>12</td>
<td>9</td>
<td>-106 @ 1MHz</td>
<td>-109 Thick metal (2.1 µm) and field oxide (11µm)</td>
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<td>[Razav ISSCC97]</td>
<td>0.6-um CMOS</td>
<td>1.8</td>
<td>15</td>
<td>7</td>
<td>-100 @ 500kHz</td>
<td>-102 Linear tuning; quadrature signals</td>
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<td>[Dauph ISSCC97]</td>
<td>11-GHz BiCMOS</td>
<td>1.5</td>
<td>40</td>
<td>10</td>
<td>-105 @ 100kHz</td>
<td>-119 Hollow rectangular coils standard process</td>
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<td>[Janse ISSCC97]</td>
<td>15-GHz Bip</td>
<td>2.2</td>
<td>43</td>
<td>11</td>
<td>-99 @ 100kHz</td>
<td>-116 High-Q MIS capacitor and varactor</td>
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<tr>
<td>[Parke CICC97]</td>
<td>0.6-um CMOS</td>
<td>1.6</td>
<td>NA</td>
<td>12</td>
<td>-105 @ 200kHz</td>
<td>-114 Full PLL circuit; capacitor bank for extended tuning</td>
</tr>
</tbody>
</table>

### Presented designs

<table>
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<tr>
<th>Reference</th>
<th>Technology [-]</th>
<th>Freq. [GHz]</th>
<th>Power [mW]</th>
<th>Tuning [%]</th>
<th>Phase noise [dBc/Hz]</th>
<th>Remarks</th>
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<tbody>
<tr>
<td>[Steya EL94]</td>
<td>6-GHz Bip</td>
<td>1.1</td>
<td>1</td>
<td>0</td>
<td>-75 @ 10kHz</td>
<td>-106 Bonding wire inductor</td>
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<td>[Crani JSSC95]</td>
<td>0.7-um CMOS</td>
<td>1.8</td>
<td>24</td>
<td>5</td>
<td>-115 @ 200kHz</td>
<td>-124 Bonding wire inductor; enhanced LC-tank</td>
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<td>[Crani JSSC97]</td>
<td>0.7-um CMOS</td>
<td>1.8</td>
<td>6</td>
<td>14</td>
<td>-116 @ 600kHz</td>
<td>-116 2-level metal; conductive substrate; standard CMOS</td>
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<tr>
<td>[Crani CICC97]</td>
<td>0.4-um CMOS</td>
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<td>11</td>
<td>20</td>
<td>-113 @ 200kHz</td>
<td>-122 2-level metal; standard CMOS</td>
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</tbody>
</table>


[Based ESSC94] P. Basedau and Q. Huang, "A 1-GHz, 1.5-V monolithic LC oscillator in 1-μm CMOS", in *Proc. of the 1994 European


Janse ISSCC97  B. Jansen, K. Negus, and D. Lee, "Silicon bipolar VCO family for 1.1 to 2.2 GHz with fully integrated tank and tuning circuits", in *ISSCC Digest of Technical Papers*, San Fransisco, USA, February 1997, pp. 392-393.


